6.4.1. Switch stress and switch utilization

- Largest single cost in a converter is usually the cost of the active semiconductor devices
- Conduction and switching losses associated with the active semiconductor devices often dominate the other sources of loss

This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices.

Minimization of total switch stresses leads to reduced loss, and to minimization of the total silicon area required to realize the power devices of the converter.

Total active switch stress S

In a converter having k active semiconductor devices, the total active switch stress S is defined as

$$S = \sum_{j=1}^{k} V_j I_j$$

where

V_j is the peak voltage applied to switch j,

I_j is the rms current applied to switch j (peak current is also sometimes used).

In a good design, the total active switch stress is minimized.

Active switch utilization U

It is desired to minimize the total active switch stress, while maximizing the output power P_{load}.

The active switch utilization U is defined as

$$U = \frac{P_{load}}{S}$$

The active switch utilization is the converter output power obtained per unit of active switch stress. It is a converter figure-of-merit, which measures how well a converter utilizes its semiconductor devices.

Active switch utilization is less than 1 in transformer-isolated converters, and is a quantity to be maximized.

Converters having low switch utilizations require extra active silicon area, and operate with relatively low efficiency.

Active switch utilization is a function of converter operating point.

CCM flyback example: Determination of S

During subinterval 2, the transistor blocks voltage $V_{Q1,pk}$ equal to V_g plus the reflected load voltage:

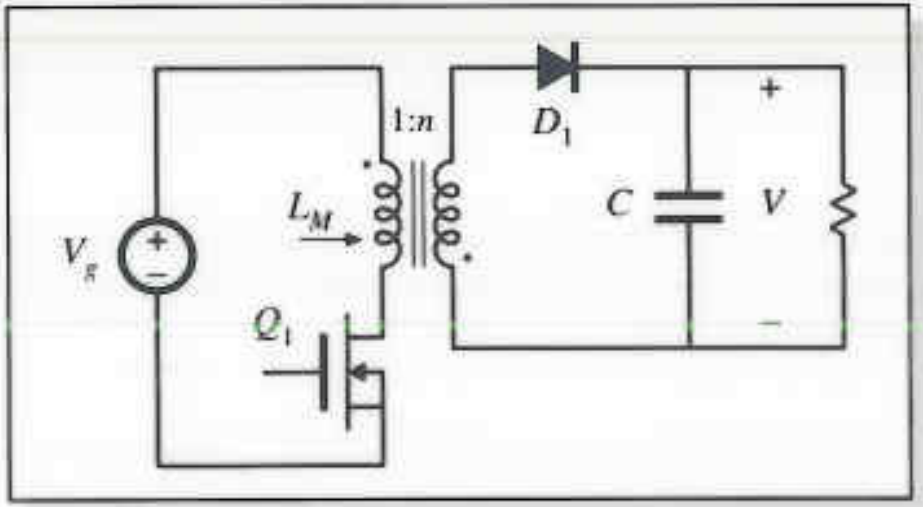
$$V_{Q1,pk} = V_g + \frac{V}{n} = \frac{V_g}{D'}$$

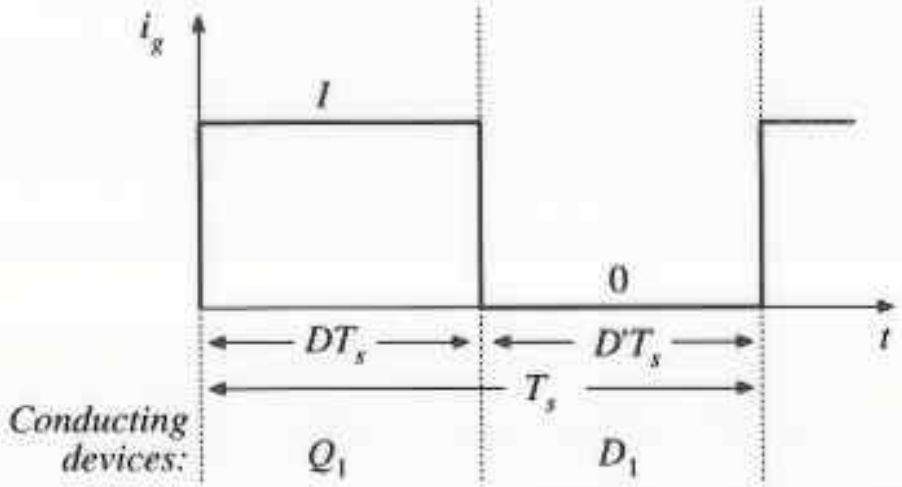
Transistor current coincides with $i_g(t)$. RMS value is

$$I_{Q1,rms} = I\sqrt{D} = \frac{P_{load}}{V_g\sqrt{D}}$$

Switch stress S is

$$S = V_{Q1,pk}\, I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right)$$





CCM flyback example: Determination of U

Express load power P_{load} in terms of V and I:

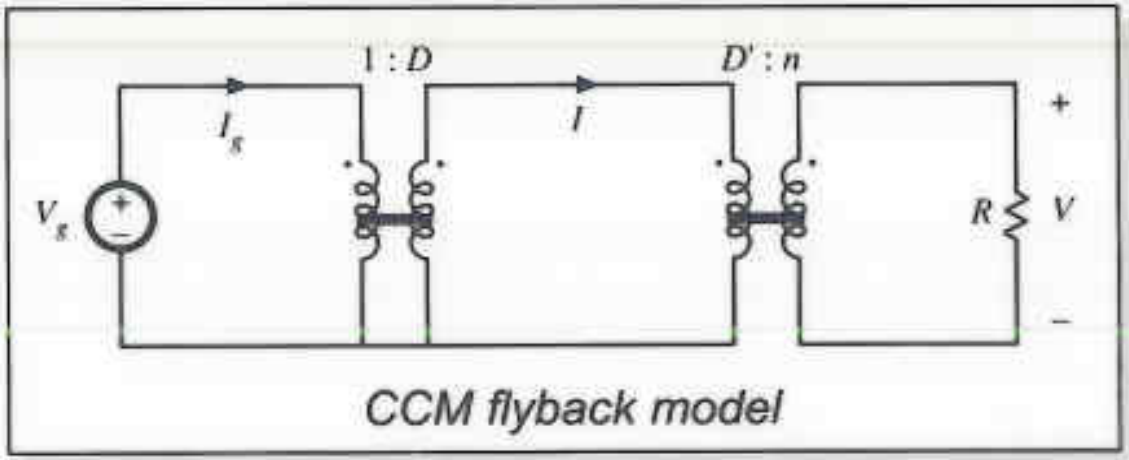
$$P_{load} = D' V \frac{I}{n}$$

Previously-derived expression for S:

$$S = V_{Q1,pk} I_{Q1,rms} = \left(V_g + \frac{V}{n} \right) \left(I \sqrt{D} \right)$$

Hence switch utilization U is

$$U = \frac{P_{load}}{S} = D' \sqrt{D}$$



CCM flyback model

Flyback example: switch utilization $U(D)$

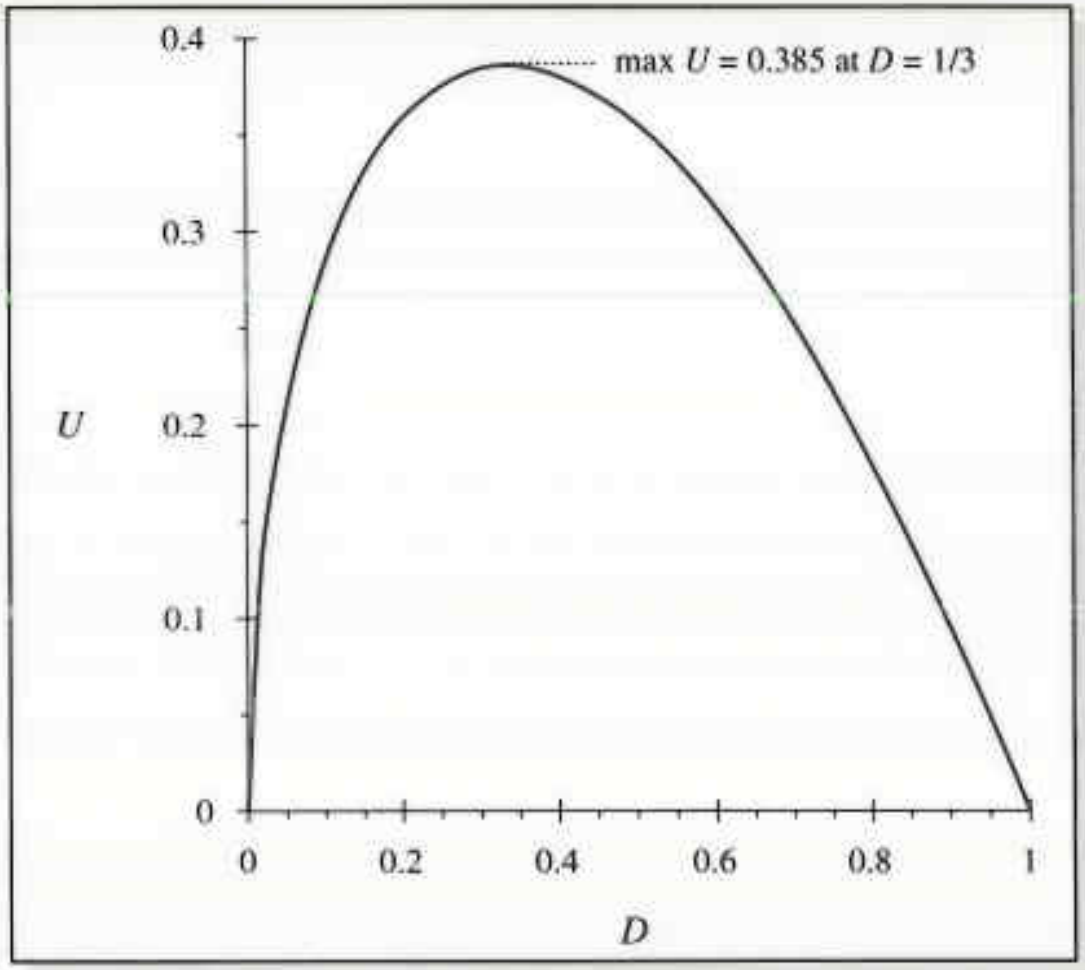
For given V, V_g, P_{load}, the designer can arbitrarily choose D. The turns ratio n must then be chosen according to

$$n = \frac{V}{V_g}\frac{D'}{D}$$

Single operating point design: choose $D = 1/3$.

small D leads to large transistor current

large D leads to large transistor voltage



Comparison of switch utilizations of some common converters

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

Converter	$U(D)$	max $U(D)$	max $U(D)$ *occurs at* $D =$
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full-bridge, half-bridge, push-pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full bridge, push-pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Switch utilization : Discussion

- Increasing the range of operating points leads to reduced switch utilization
- Buck converter
  - can operate with high switch utilization (U approaching 1) when D is close to 1
- Boost converter
  - can operate with high switch utilization (U approaching ∞) when D is close to 1
- Transformer isolation leads to reduced switch utilization
- Buck-derived transformer-isolated converters
  - $U \leq 0.353$
  - should be designed to operate with D as large as other considerations allow
  - transformer turns ratio can be chosen to optimize design

Switch utilization: Discussion

- Nonisolated and isolated versions of buck-boost, SEPIC, and Cuk converters
  - $U \leq 0.385$
  - Single-operating-point optimum occurs at $D = 1/3$
  - Nonisolated converters have lower switch utilizations than buck or boost
  - Isolation can be obtained without penalizing switch utilization

Active semiconductor cost vs. switch utilization

$$\left(\begin{array}{c}\text{semiconductor cost}\\ \text{per kW output power}\end{array}\right) = \frac{\left(\begin{array}{c}\text{semiconductor device cost}\\ \text{per rated kVA}\end{array}\right)}{\left(\begin{array}{c}\text{voltage}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{current}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{converter}\\ \text{switch}\\ \text{utilization}\end{array}\right)}$$

(semiconductor device cost per rated kVA) = cost of device, divided by product of rated blocking voltage and rms current, in \$/kVA. Typical values are less than \$1/kVA

(voltage derating factor) and (current derating factor) are required to obtain reliable operation. Typical derating factors are 0.5 - 0.75

Typical cost of active semiconductor devices in an isolated dc-dc converter: \$1 - \$10 per kW of output power.

Summary of key points

1. The boost converter can be viewed as an inverse buck converter, while the buck-boost and Cuk converters arise from cascade connections of buck and boost converters. The properties of these converters are consistent with their origins. Ac outputs can be obtained by differential connection of the load. An infinite number of converters are possible, and several are listed in this chapter.

2. For understanding the operation of most converters containing transformers, the transformer can be modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing inductance must obey all of the usual rules for inductors, including the principle of volt-second balance.

Summary of key points

3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.

4. In the full-bridge, half-bridge, and push-pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.

Summary of key points

5. In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.
6. The flyback converter is based on the buck-boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.
7. The transformer turns ratio is an extra degree-of-freedom which the designer can choose to optimize the converter design. Use of a computer spreadsheet is an effective way to determine how the choice of turns ratio affects the component voltage and current stresses.
8. Total active switch stress, and active switch utilization, are two simplified figures-of-merit which can be used to compare the various converter circuits.