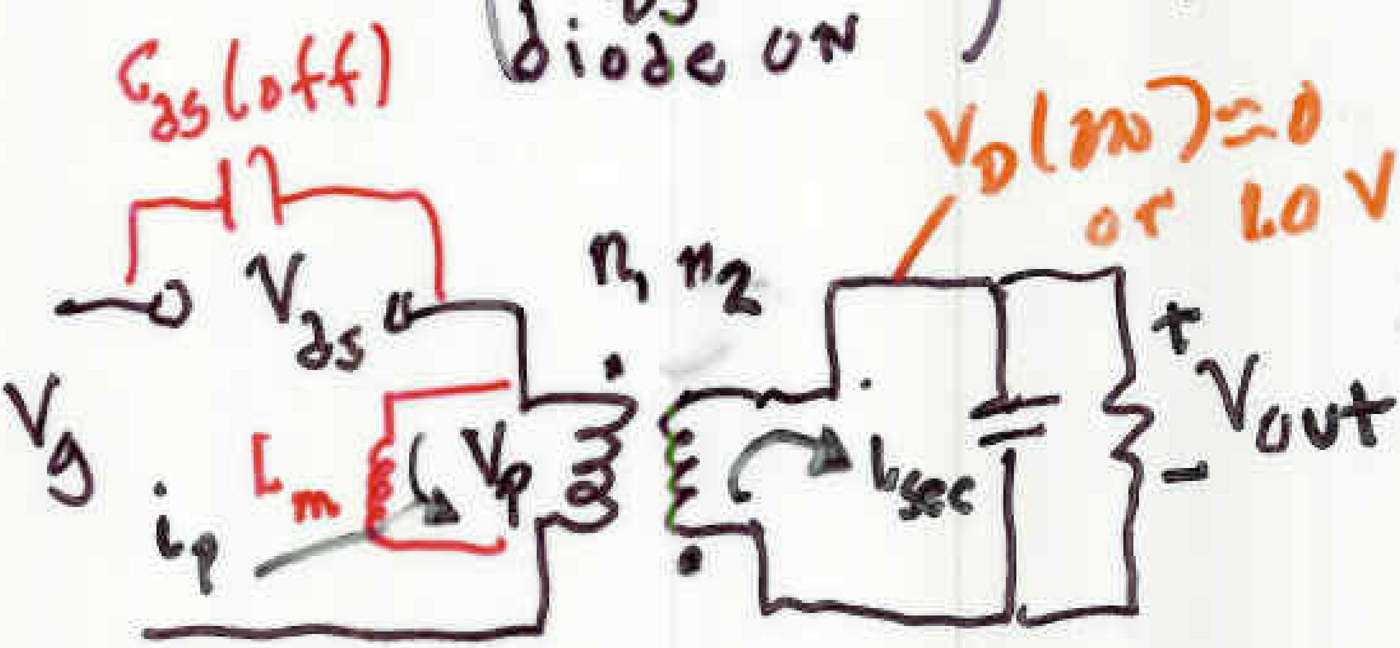
Q stress ($V_{DS}(off)$ diode ON): Flyback



$$|V_p| = \left(\frac{V_o}{n_2}\right) n_1 \quad \begin{matrix} - \\ \text{polarity} \\ + \end{matrix}$$

fine tune

$$+V_g \text{ —o} \quad \text{o— } -\frac{V_o}{n_2}n_1 - V_D(on)\frac{n_1}{n_2}$$

V_p from secondary

$V_{ds}(t)$

$V_g + (V_o + V_D)\frac{n_1}{n_2}$

Worst case?

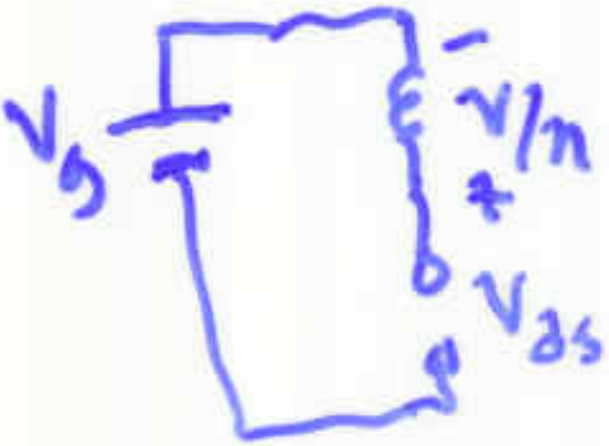
Soon Ch 19

L_ℓ can cause ringing with $C_{ds}(off)$ oh no see V_{pk}

Intro to Pbm 6.4

$V_{ds}(off)$ stress is worst case (w.o. L_ℓ) $= V_g + \frac{V}{n}$

$C_{ds(off)}$



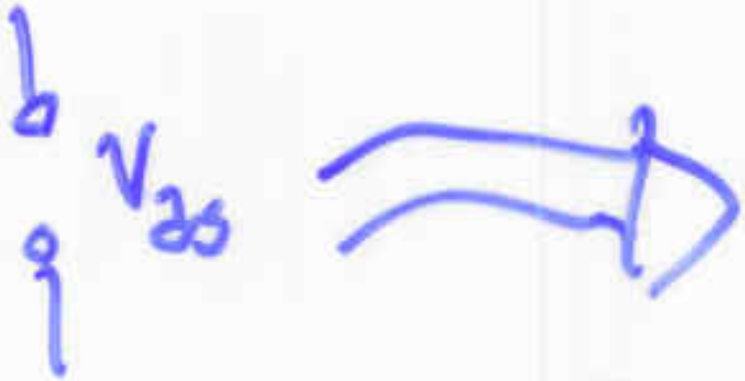
L_ℓ (leakage) exists ; Next level

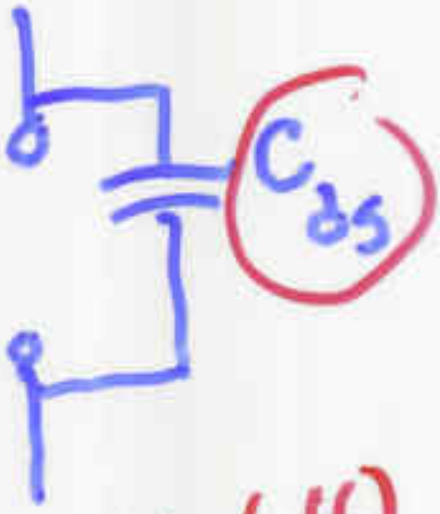
$V_\ell = L_\ell \, di/dt$

$V_{ds}(off) = V_g + \frac{V}{n} + V_\ell$

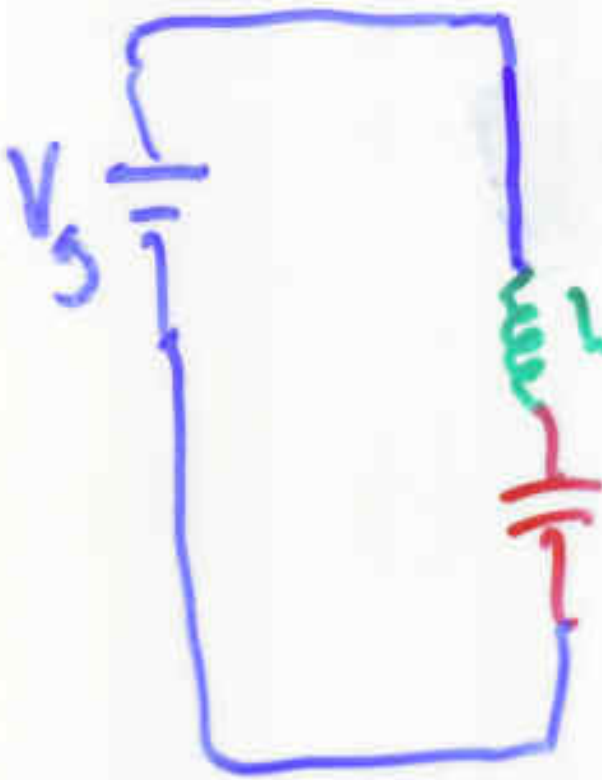
$V_{ds}(off)$ is correct?

Next next level





Series resonance



No Ch 19

changes to

$V_{ds(peak)}$ Kills FET

Ch 19

Ring causes Emc noise!

cannot pass compliance

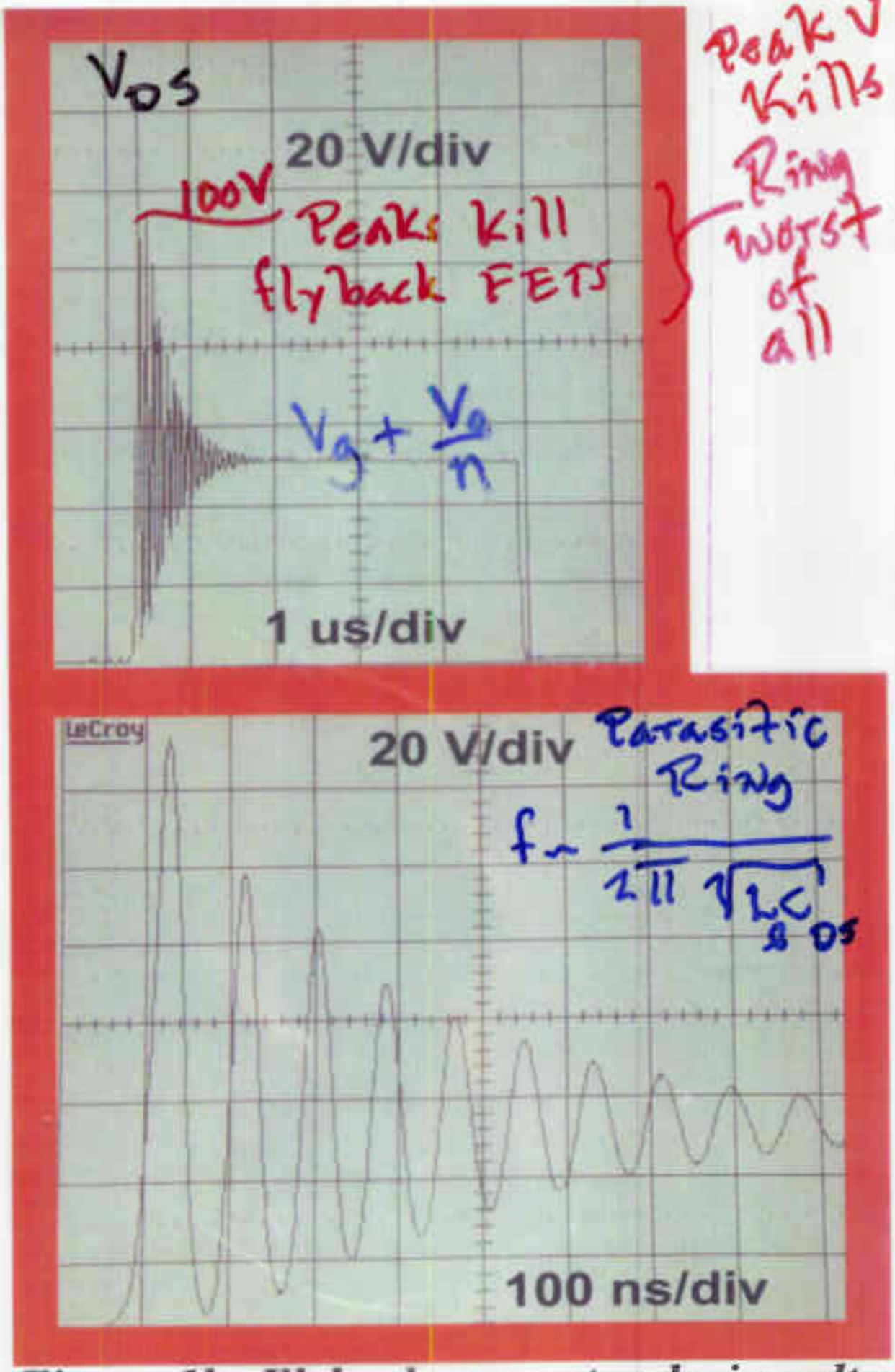


Figure 1b: Flyback converter drain voltage with no snubber

How to reduce ringing?

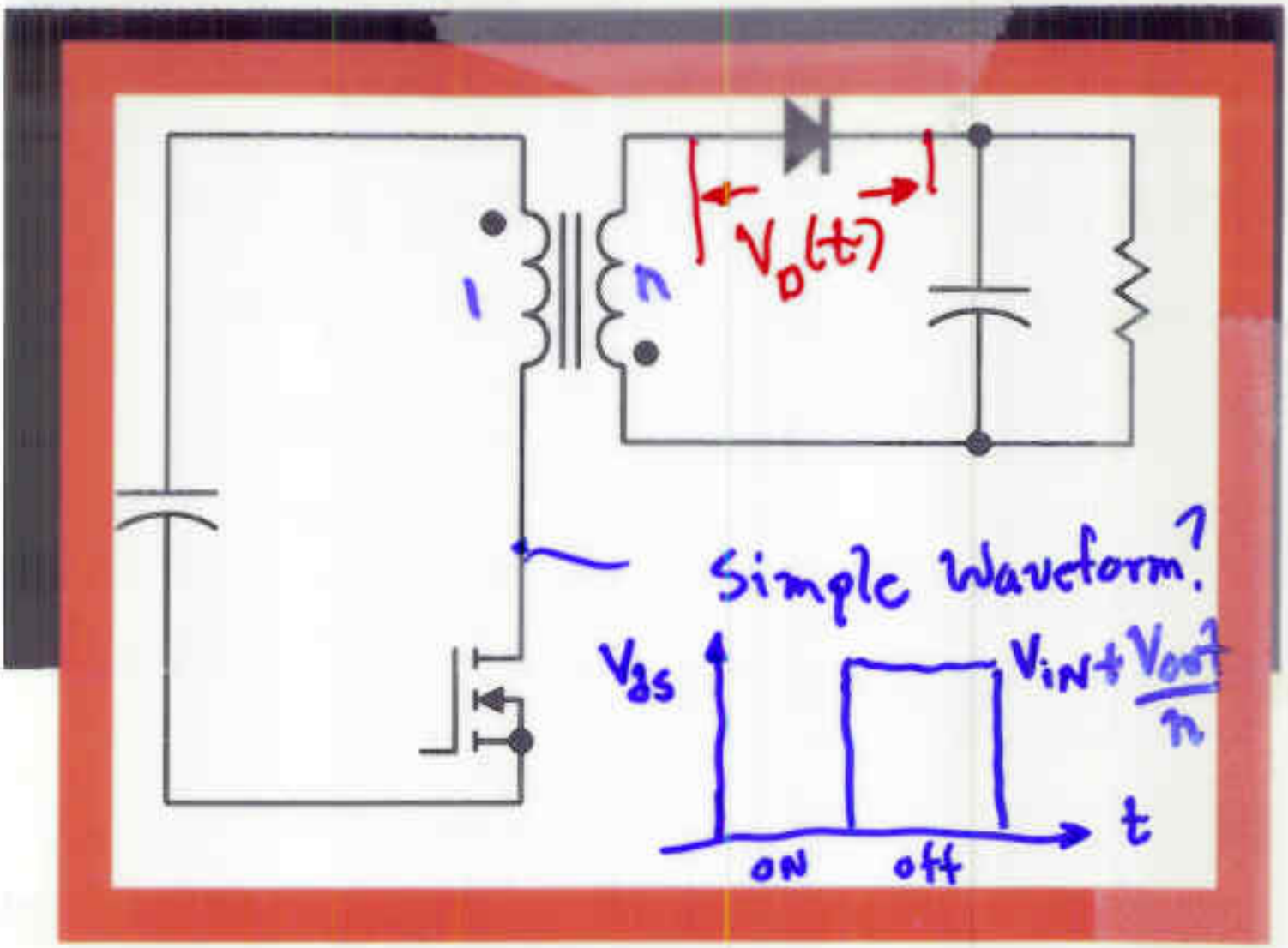


Figure 1a: Flyback converter schematic

What about L (leakage) in series

it stores $\frac{1}{2} I_{PK}^2 L$ when FET is ON

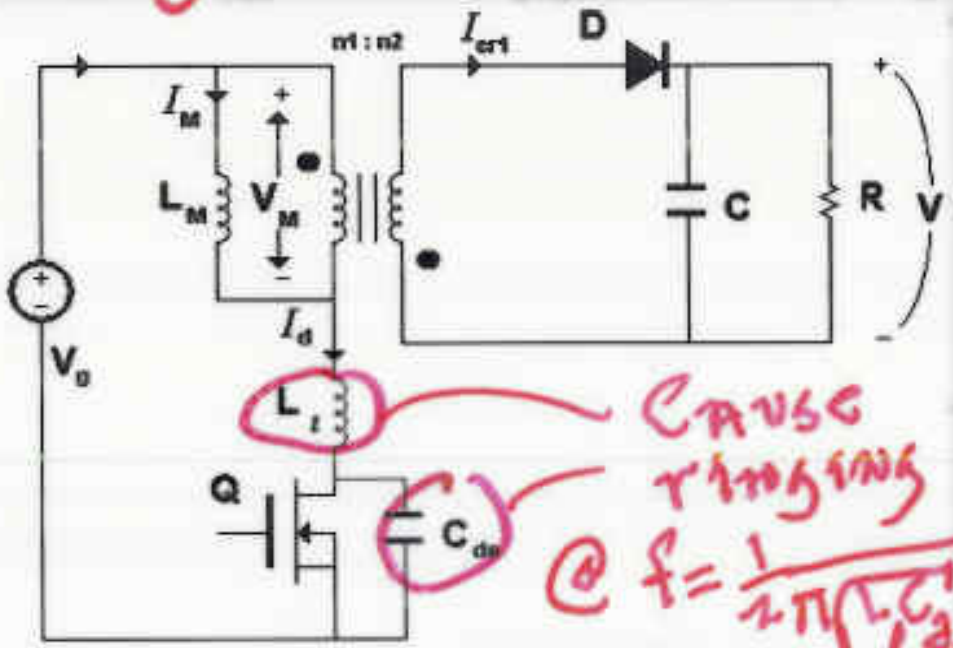
FET goes off this energy "rings"

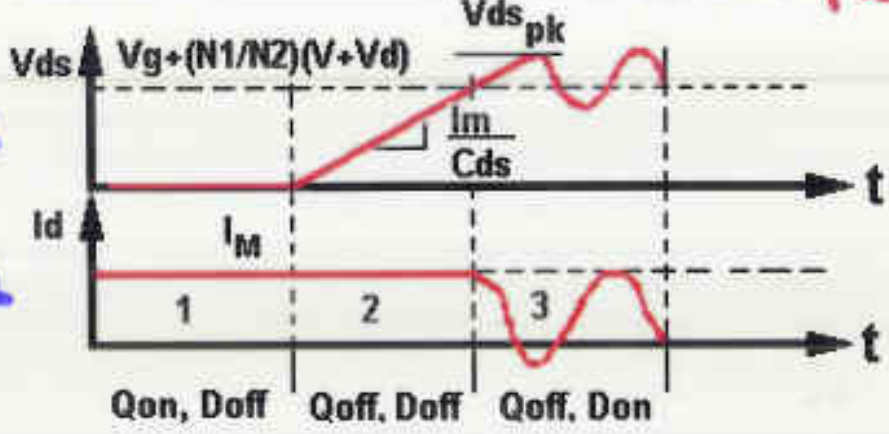
$C_{DS}(off)$

via

L_e ← 563

Transistor stress in flyback converter





Vdspk it happens when Q turns OFF

D turns on only on interval 3 and remains reversed biased as long as :
$(Vg-Vds)(N2/N1) > V$

The average power loss Ps for parasitic elements L_L and Cds is

$Ps=1/2 L_L I^2_M f_s$

Transistor voltage peak Vdspk is:

$Vdspk=Vg+(N1/N2)(V+Vd)+(D/D'^2)(Ro/R)Vg$

$Ro=(L_L/Cds)^{1/2}$

The oscillation frequency for the over-voltage is determined by L_L and Cds

Choices FET with C_{ds}

Trf with L_l

Consequences

One fix is use two Q in series driven the same

$V_{gs}(off)$ effects $\div 2$

Second fix Clamp primary