6.4. Converter evaluation and design

For a given application, which converter topology is best?

There is no ultimate converter, perfectly suited for all possible applications

Trade studies

- Rough designs of several converter topologies to meet the given specifications
- An unbiased quantitative comparison of worst-case transistor currents and voltages, transformer size, etc.

Comparison via switch stress, switch utilization, and semiconductor cost

Spreadsheet design

6.4.2. Converter design using computer spreadsheet

Given ranges of V_g and P_{load}, as well as desired value of V and other quantities such as switching frequency, ripple, etc., there are two basic engineering design tasks:

- Compare converter topologies and select the best for the given specifications
- Optimize the design of a given converter

A computer spreadsheet is a very useful tool for this job. The results of the steady-state converter analyses of Chapters 1-6 can be entered, and detailed design investigations can be quickly performed:

- Evaluation of worst-case stresses over a range of operating points
- Evaluation of design tradeoffs

Spreadsheet design example

Choices

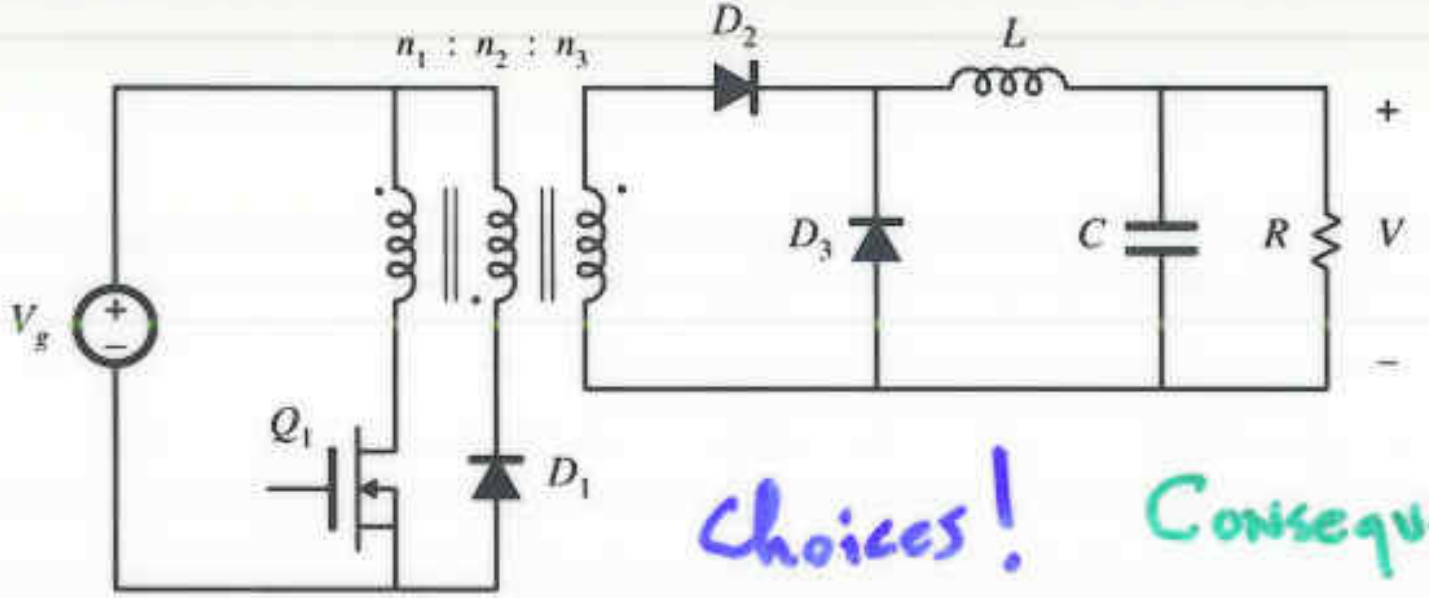
Specifications	
Maximum input voltage V_g	390 V
Minimum input voltage V_g	260 V
Output voltage V	15 V
Maximum load power P_{load}	200 W
Minimum load power P_{load}	20 W
Switching frequency f_s	100 kHz
Maximum output ripple Δv	0.1 V

- Input voltage: rectified 230 Vrms ±20%
- Regulated output of 15 V
- Rated load power 200 W
- Must operate at 10% load
- Select switching frequency of 100 kHz
- Output voltage ripple ≤ 0.1V

Compare single-transistor forward and flyback converters in this application

Specifications are entered at top of spreadsheet

Forward converter design, CCM



Choices!

Consequences?

Design variables

Reset winding turns ratio n_2 / n_1	1
Turns ratio n_3 / n_1	0.125
Inductor current ripple Δi	2A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Enter results of converter analysis into spreadsheet (Forward converter example)

Maximum duty cycle occurs at minimum V_g and maximum P_{load}. Converter then operates in CCM, with

$$D = \frac{n_1}{n_3} \frac{V}{V_g}$$

Inductor current ripple is

$$\Delta i = \frac{D'VT_s}{2L}$$

Solve for L:

$$L = \frac{D'VT_s}{2\Delta i}$$

Consequence #1

Δi is a design variable. For a given Δi, the equation above can be used to determine L. To ensure CCM operation at full load, Δi should be less than the full-load output current. C can be found in a similar manner.

Forward converter example, continued

Check for DCM at light load. The solution of the buck converter operating in DCM is

$$V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + \frac{4K}{D^2}}}$$

with $K = 2L / R T_s$, and $R = V^2 / P_{load}$

These equations apply equally well to the forward converter, provided that all quantities are referred to the transformer secondary side.

Solve for D:

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2n_3 V_g}{n_1 V} - 1\right)^2 - 1}} \quad \text{in DCM}$$

$$D = \frac{n_1}{n_3} \frac{V}{V_g} \quad \text{in CCM}$$

at a given operating point, the actual duty cycle is the small of the values calculated by the CCM and DCM equations above. Minimum D occurs at minimum P_{load} and maximum V_g.

More regarding forward converter example

Worst-case component stresses can now be evaluated.

Peak transistor voltage is

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

RMS transistor current is

$$I_{Q1,rms} = \frac{n_3}{n_1}\sqrt{D}\sqrt{I^2 + \frac{\left(\Delta i\right)^2}{3}} \approx \frac{n_3}{n_1}\sqrt{D}\, I$$

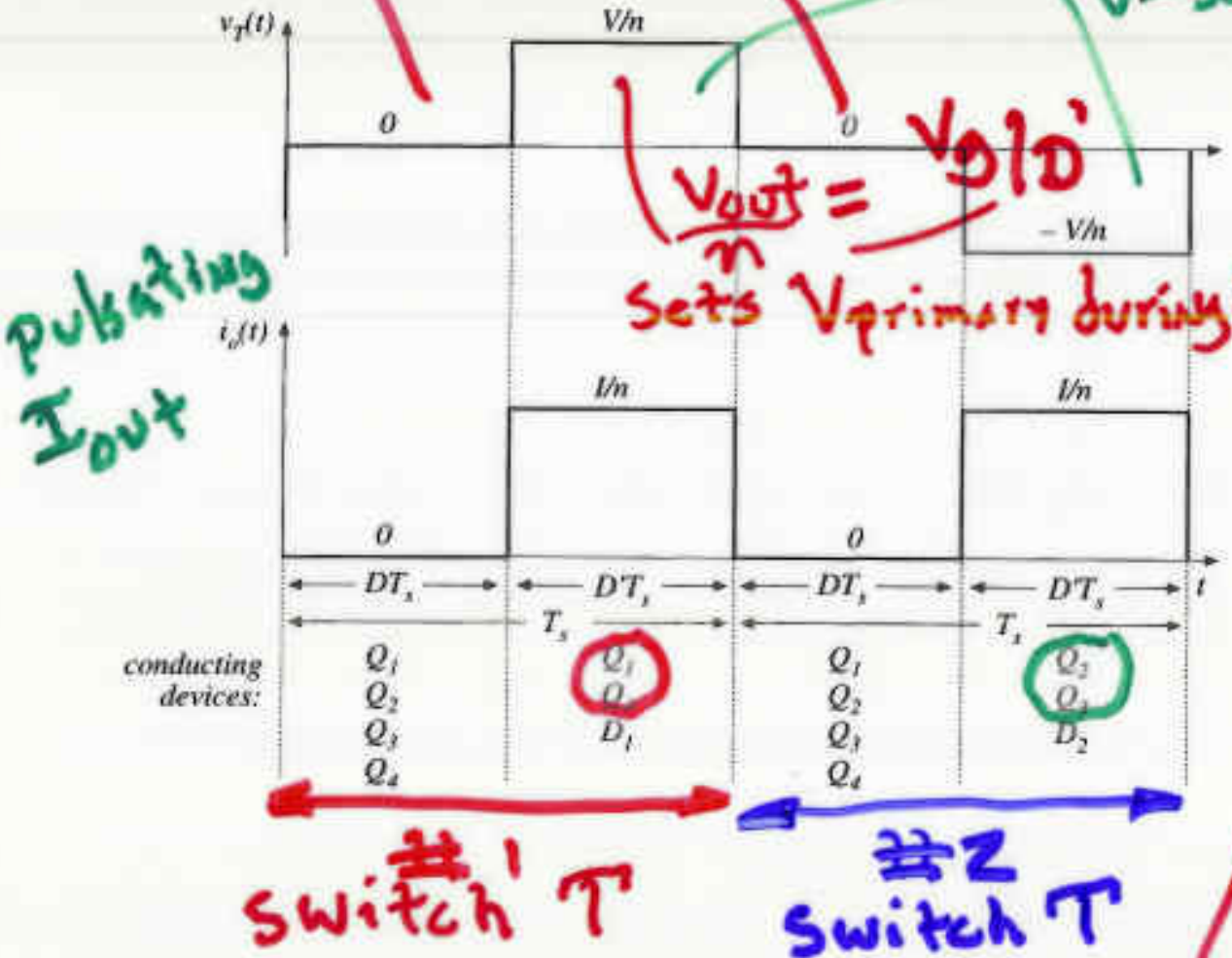
(this neglects transformer magnetizing current)

Other component stresses can be found in a similar manner.
Magnetics design is left for a later chapter.

How to force $V_{prim} = 0$? $V_p = 0 \Rightarrow V_g = $ light

Transformer reset mechanism

Equal/Opposite V-sec



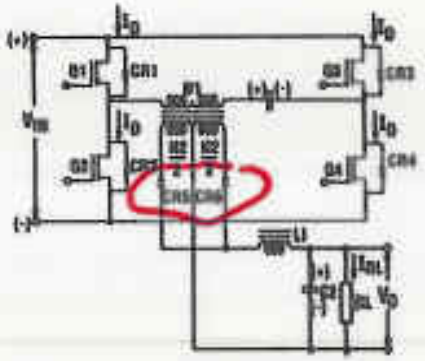
- As in full-bridge buck topology, transformer volt-second balance is obtained over two switching periods. Key
- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s, applying volt-seconds VDT_s to secondary winding.
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s, applying volt-seconds $-VDT_s$ to secondary winding.

Pro-active Core Reset Methodology

TYPE OF CONVERTER

Full Bridge

CIRCUIT CONFIGURATION



$\frac{V_{IN}}{N_1} = \frac{V_O}{\frac{N_2}{2}}$

IDEAL TRANSFER FUNCTION

$$\frac{V_O}{V_{IN}} = 2\frac{N_2}{N_1}\left(\frac{t_{on}}{T_S}\right) = 2\frac{N_2}{N_1}(D)$$

PEAK DRAIN CURRENT •

$$I_{DMAX} = \frac{N_2}{N_1}\left(I_{RL} + \frac{\Delta I_L}{2}\right) + I_{MAG}$$

(I_{MAG} = Peak magnetizing current.)

PEAK DRAIN VOLTAGE •

$$V_{DS} = V_{IN}$$

AVERAGE DIODE CURRENTS •

$$I_{CR5} = I_{RL}$$

$$I_{CR6} = I_{RL}$$

Big DZI for small Δi

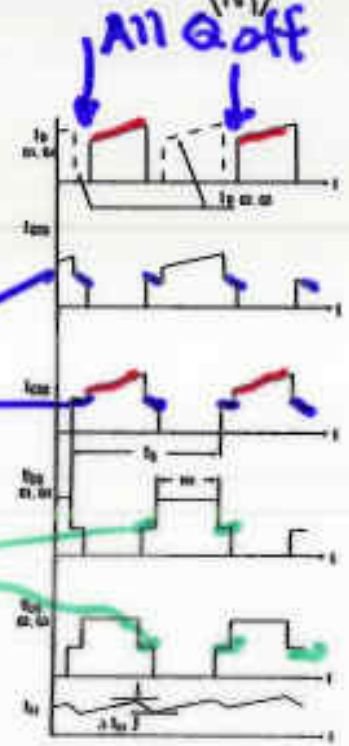
$I_{diode\ AV} = I_{ON}^{AV} D + D' I_{off}^{AV}$

staircase max = I_{RL}

DIODE VOLTAGES (VRM) •

$$V_{RM}\begin{cases} V_{CR5} = 2V_{IN}\left(\frac{N_2}{N_1}\right)V_{CR1} = V_{IN} \\ V_{CR6} = 2V_{IN}\left(\frac{N_2}{N_1}\right)V_{CR2} = V_{IN} \end{cases}$$

VOLTAGE AND CURRENT WAVEFORMS



ADVANTAGES

Good transformer utilization, transistors rated at V_{IN}, isolation, multiple outputs. ID is reduced as a ratio of N_2/N_1. Zero voltage switching possible Low output ripple.

DISADVANTAGES

High parts count. C1 has high ripple current. Requires high side switch drive. Cross conduction of Q1 and Q2 or Q3 and Q4 possible. High input current ripple.

TYPICAL APPLICATIONS

High power, high input voltage

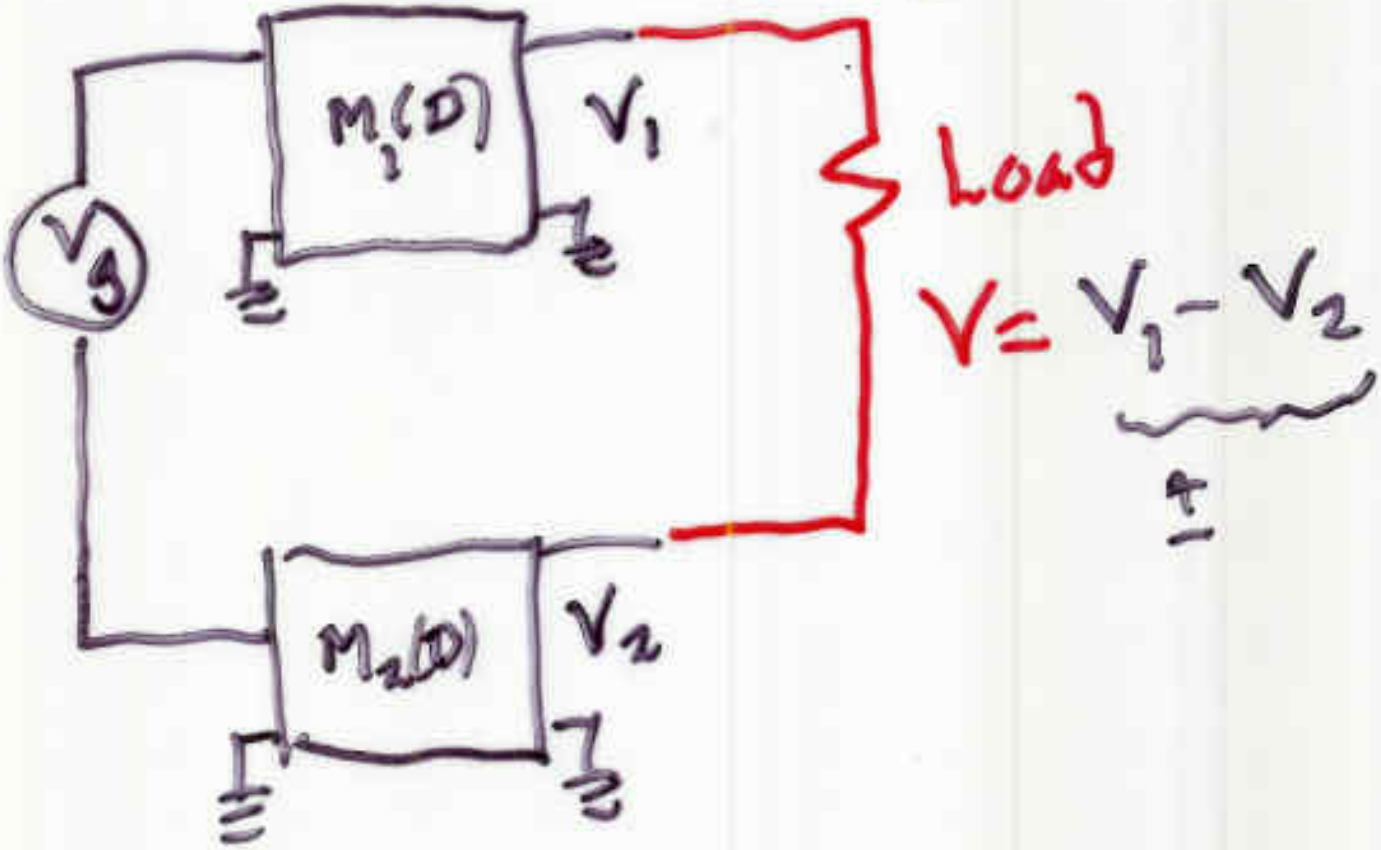
APPLICABLE HARRIS PRODUCTS

HIP4080/81 HIP2500 HV400

Summary of key points

3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.
4. In the full-bridge, half-bridge, and push-pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.

Differential Output

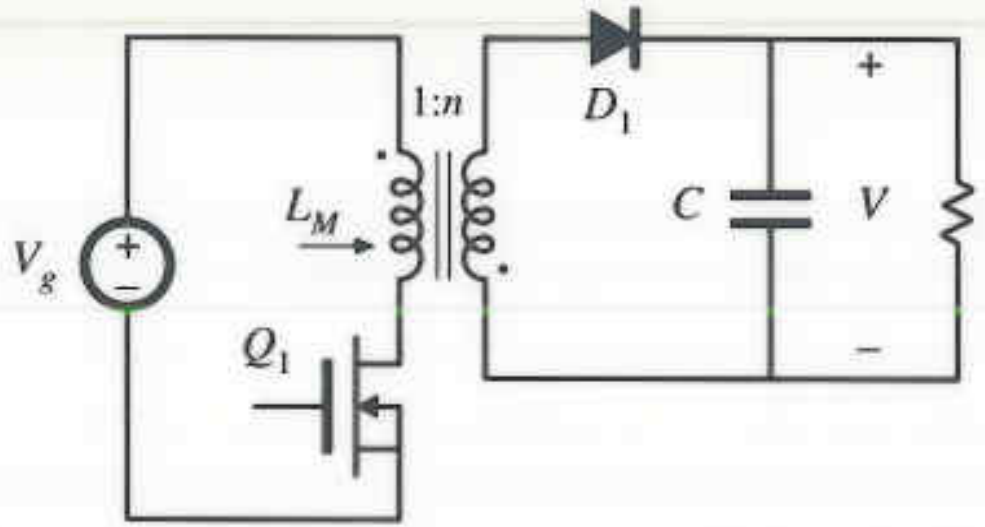


Case $M_1(D)$ buck driven by D

$M_2(D')$ buck driven by D'

$$V_{out} = DV_g - D'V_g = (2D-1)V_g$$

Flyback converter design, CCM



Design variables

Turns ratio n_2 / n_1	0.125
Inductor current ripple Δi	3 A ref to sec

- Design for CCM at full load; may operate in DCM at light load