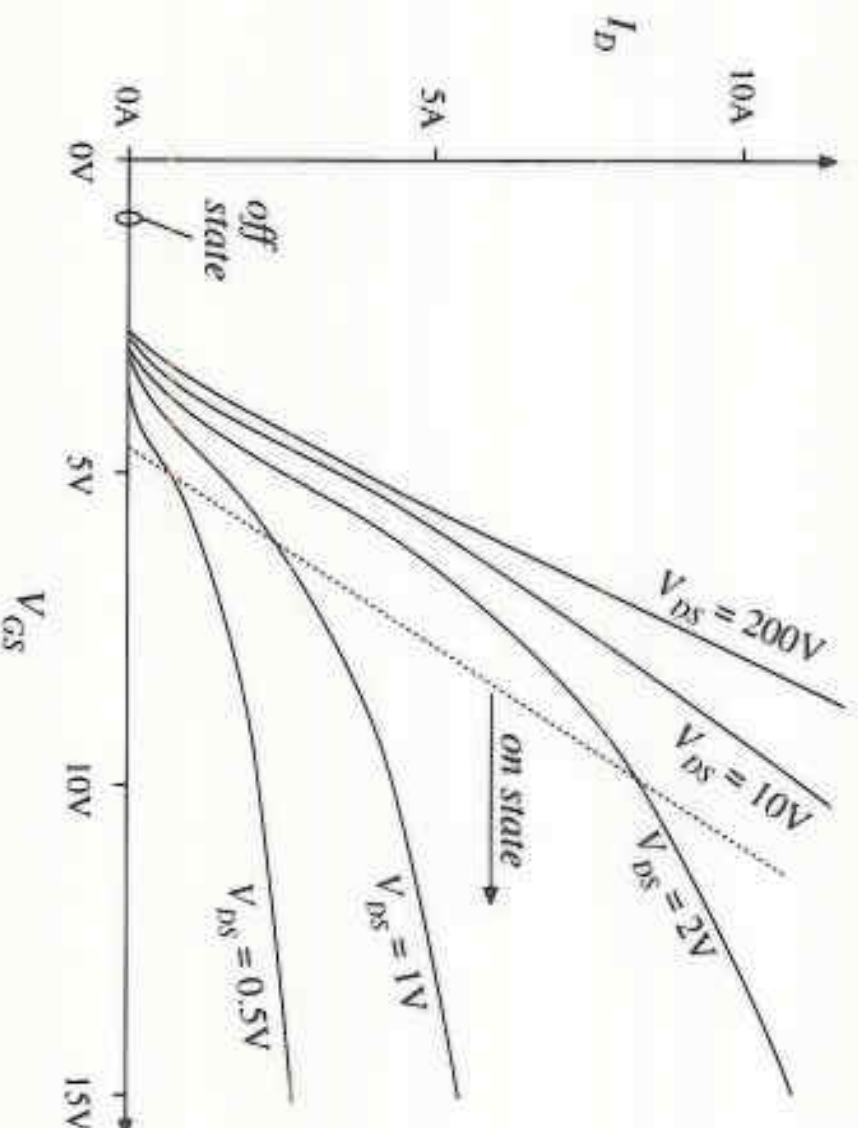


Fig. 1. As shown in this generalized graph of output characteristics, an n-channel power MOSFET has three possible modes of operation.

Typical MOSFET characteristics

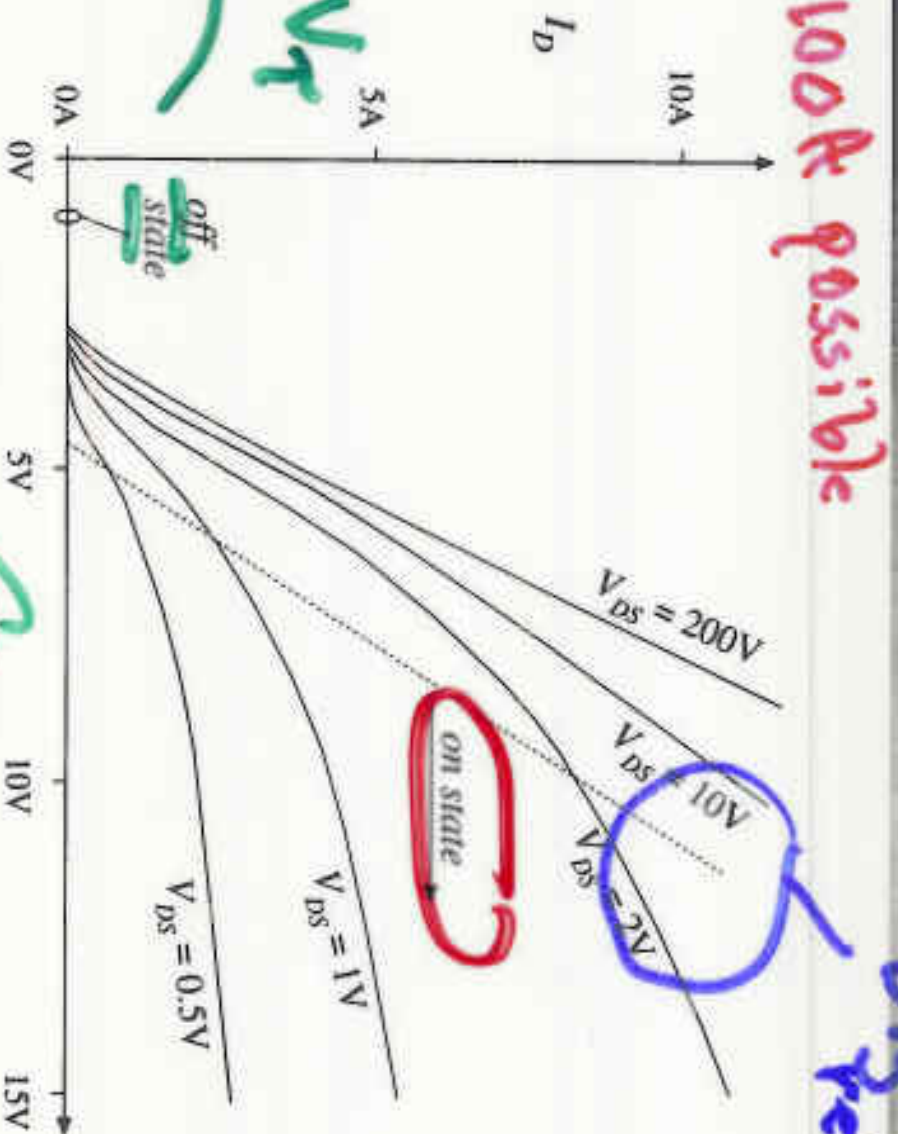


- Off state: $V_{GS} < V_{th}$
- On state: $V_{GS} \gg V_{th}$
- MOSFET can conduct peak currents well in excess of average current rating
—characteristics are unchanged
- on-resistance has positive temperature coefficient, hence easy to parallel

Fig 4.28

C_{in} to power FET : $10nF$
 $100nF$

Typical MOSFET characteristics



- Off state: $V_{GS} < V_{th}$
- On state: $V_{GS} \gg V_{th}$
- MOSFET can conduct peak currents well in excess of average current rating — characteristics are unchanged
- on-resistance has positive temperature coefficient, hence easy to parallel

High P corner

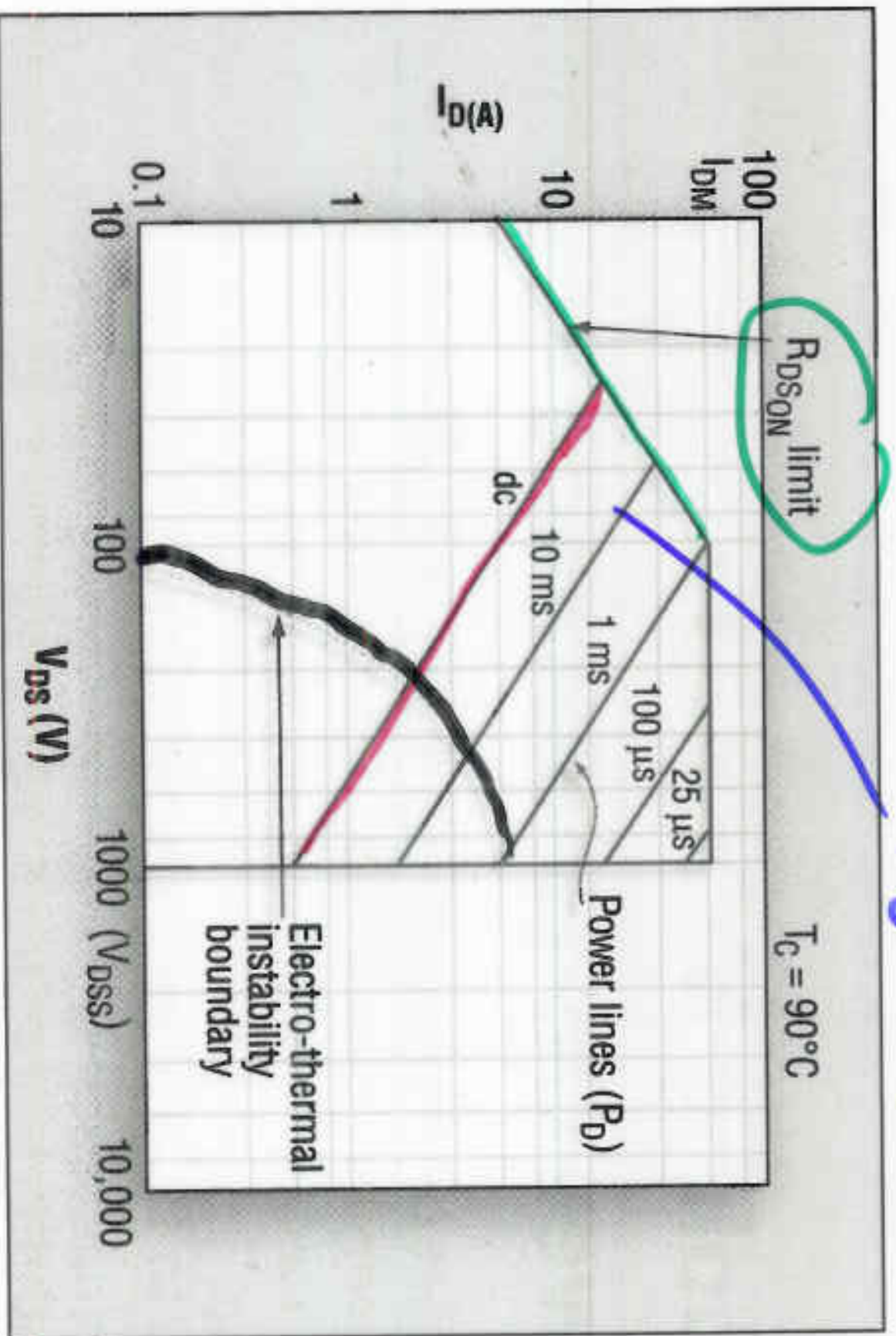


Fig. 2. Power MOSFETs optimized for switched-mode designs have limited ability to operate in the corner of the FBSOA graph, where electro-thermal instability can occur as shown here for a typical n-channel power MOSFET.

SOA

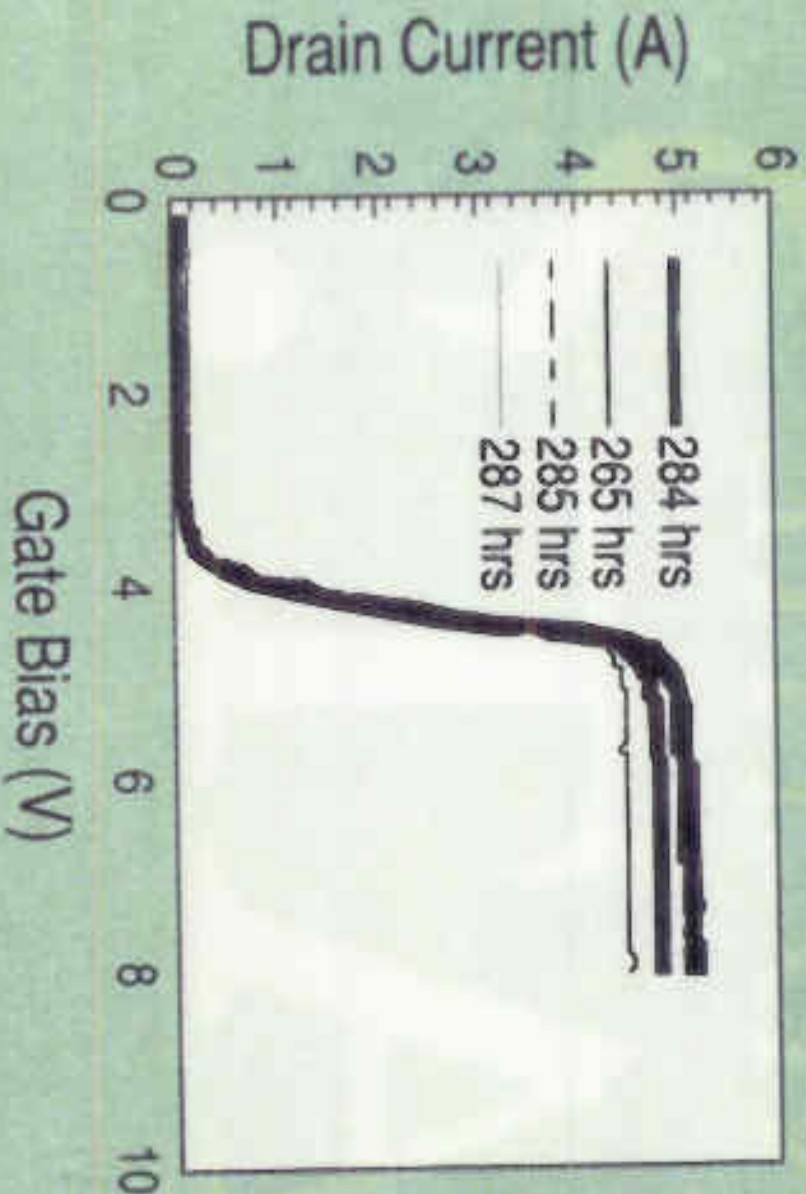


Figure 3. Degradation of MOSFET transfer curve with time under avalanche stress.

With (avalanche) stress

$R_{DS(on)} \uparrow$

$V_{GS} \uparrow$

$\therefore P_{D(av)} \uparrow$
50A

Other stress

$\frac{dV}{dt}$

reverse recovery
Qrr

Derate

High f / region

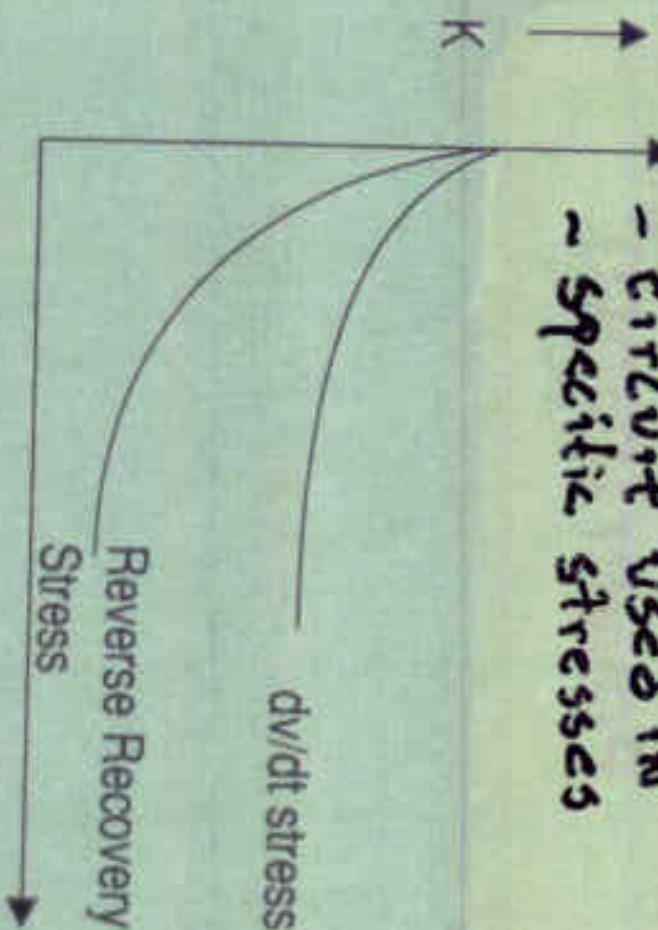
K is experimental factor

depends on:

- circuit used in
- specific stresses



(a) Dynamic SOA



(b) Variation of K with age

Figure 4. SOA characteristics.

Simple boost: Avalanche stress

Bridge: Arr from body diode

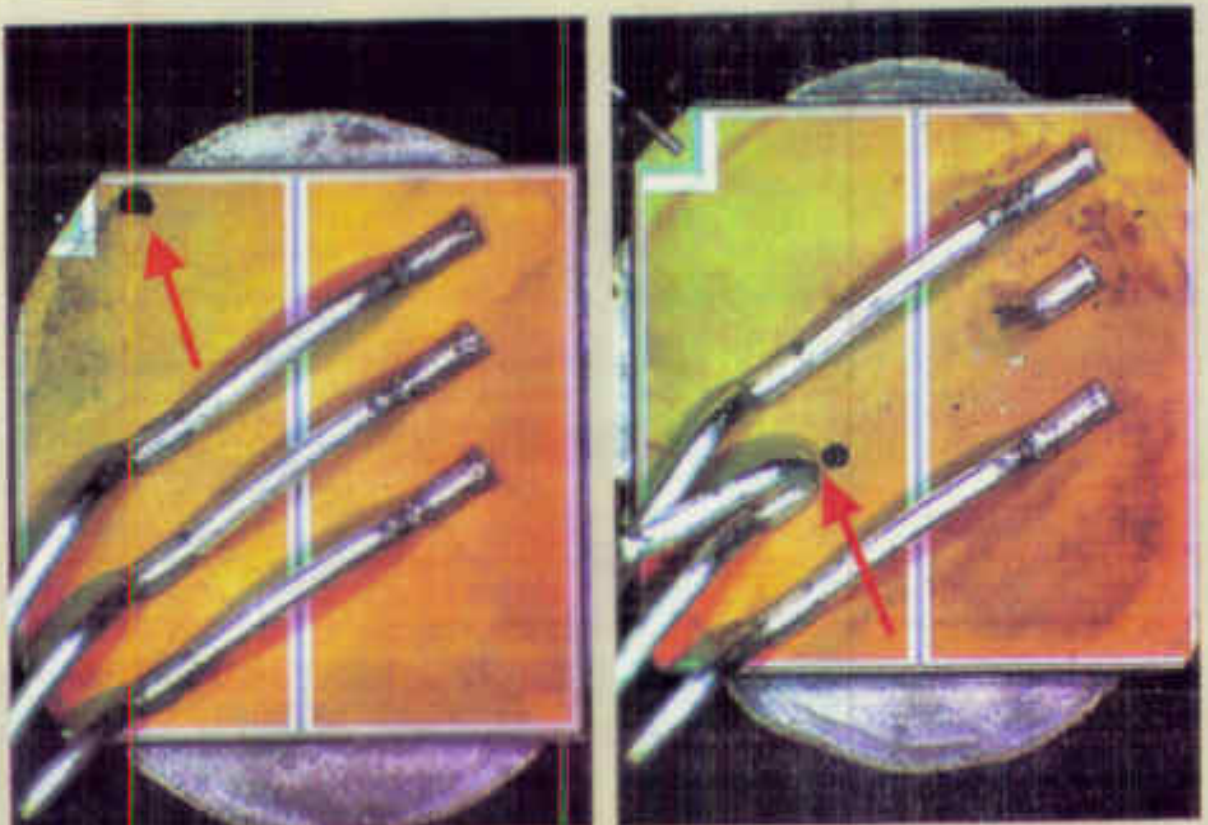
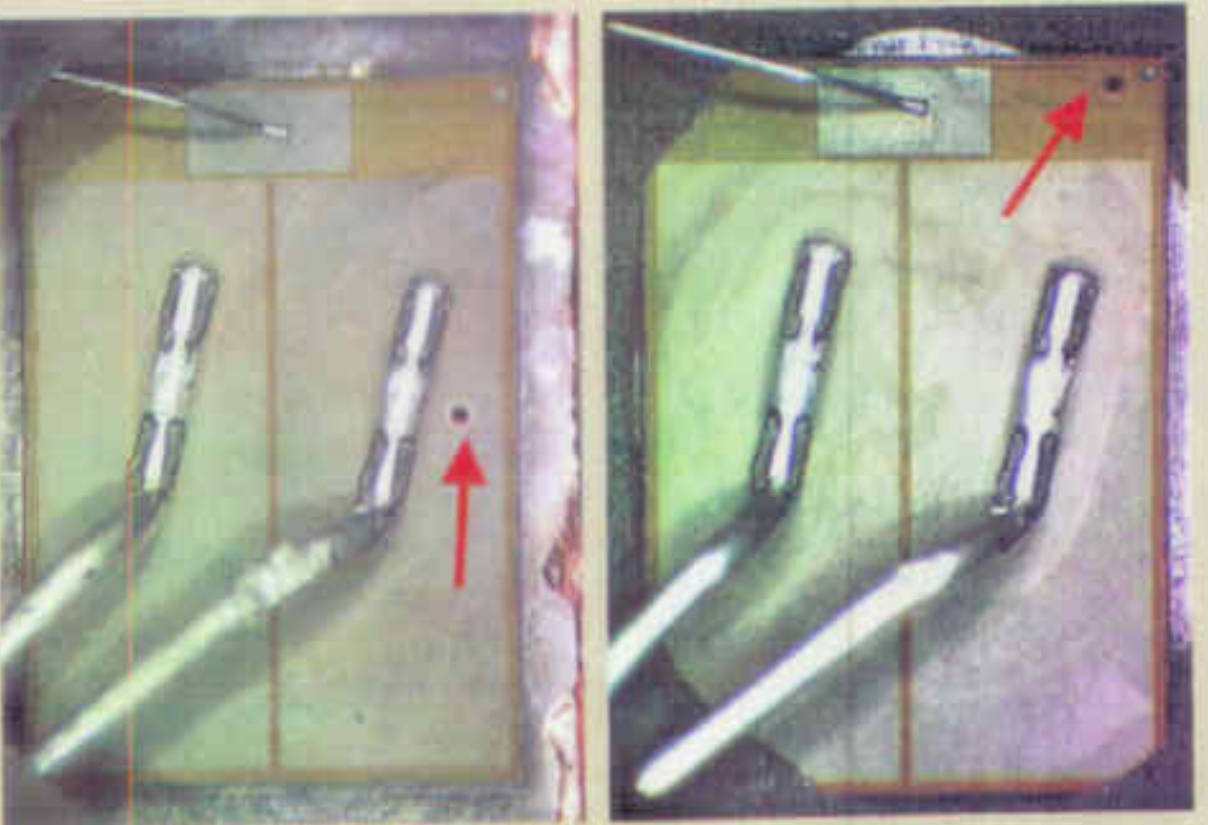


Fig. 3. Avalanche damage to Planar FETs (left) and Trench FETs (right). The bond-wire has been cut and moved out of the way to expose the damage in the part at upper right.