ECE 562  Professor. George Collins  Power Electronics

ECE562 (3 Credits)  Power Electronics

Schedule and Grading  
August 24th to Dec 10th 2015

SEE http://www.calendar.colostate.edu/

- **CLASSES BEGIN Tues. 25th August**
- Divide yourselves into groups of **FOUR** or more (limit of 6) for doing group HW, Spice Labs, Pop Quizzes and Talks # 1 and #2. Do this ASAP and give the list of group members to both me and the grader.
- **Class Time:** Tuesday and Thursday 5:30 – 6:45 PM in B105 (Engineering B wing)
- **Instructor:** Professor George Collins, Email: gcollins@engr.colostate.edu
- **Grader:** prerana.ghalsasi@gmail.com. SEND the grader (all of the following are group efforts—form a group ASAP) HW solutions, Spice labs, Pop Quiz solutions and Group Papers in WORD for both Talks
- **Class website:** http://www.engr.colostate.edu/ECE562/ and CSU calendar http://www.calendar.colostate.edu/
- Industry seminars are great—try this one from Arrow Electronics http://www.arrownac.com/offers/vision-2013/index.php

The materials in this class each year are 1/2 new. Hence I judge you should know the hidden sign “course under construction- pardon our appearance”

This course requires a lot of extra work in the beginning of the semester and a lot LESS work at the end of the semester, so you have time for other courses, finals and job interviews.

The class notes are password protected
Username: Student
Password: Power!

Please forgive this 11 page syllabus, schedule and grading missive, but there are lots of issues to cover. To keep it all clear and fresh, I will send out a weekly memo on each Monday or the prior Thursday/Friday detailing:

1. Last week’s efforts
2. This week’s efforts and what’s due that coming week (e.g. Pop Quiz #, SPICE Lab #, HW set #, talk schedule etc. etc.)
3. Next week’s efforts week and due dates for all new assignments
Disclaimer Notice: Because of the breath of power electronics each year is different. Perhaps the course should have a “under construction, pardon our appearance” sign. All items in this memo are subject to change by Prof. Collins in LATER class announcements and items are considered only a preliminary guide to the student. For example, the ECE562 classes can cover high frequency magnetics/transformers/inductors rather than more details of PWM circuits or basics of resonant converters, if strong class interest exists—each semester is unique in its class preferences in this diverse field. In week # 9 we will have a mid-semester review of past and future topics in which you are encouraged to input your desires for the remainder of the class lectures. See in class participation grade issues section.

COURSE OBJECTIVES

This course will teach students how to understand, analyze, design and better employ new commercial IC power supplies on a chip or on a board in any electronic system requiring powered DC levels different from the general DC system bus. Typically this is 6-12 additional DC levels. One illustrative commercial example is a remarkable Dialog Semiconductor product which provides, on ONE IC chip: 18 LDO( low drop out regulators) for low noise voltages needed for cell phone transceivers, two Buck converters for cell phone processors and semiconductor memory power supplies and one Boost converter for both driving LEDs for LCD screen backlighting or for the flash camera. ALL on one IC chip and driven by the on board batteries only!! Texas Instruments has similar products. This kind of chip allows for low cost cell phones employing various chips with various DC voltages all from one rail voltage. Cell phone sales are two billion per year and smart phones 600 million per year. This allows you to grasp why power management, at low cost, is on an IC chip or chips.

This course will cover the two major approaches to high efficiency DC-DC conversion in detail: Pulse width modulation and resonant converters. Both employ ideal lossless “L-C” networks and ideal lossless switches. The DC-DC PWM conversion is primarily an IC solution to point of load DC power requirement and the resonant DC-DC conversion is for high performance DC power applications at kW levels, usually implemented on PC boards with discrete components, often called BRICKS. However, some attention will be given to linear power supplies like low drop out regulators and switched capacitor supplies for a comparison to our two circuit types. Moreover LDO’s provide the lowest ripple rails for powering critical electronics devices, like transceivers and high speed serial interfaces to minimize the bit error rate (BER).

Group efforts are one big emphasis in 562. Upon leaving CSU you will work in a company in teams—the Word and PowerPoint skills you learn in presenting technical materials in 562 will be to YOUR benefit. The practice and experience of living with the “psychodrama of technical group efforts” will also benefit you personally.
ACADEMIC INTEGRITY

This course will adhere to Academic Integrity Policy of CSU General Catalog and Student Conduct code. It is expected in this course that all students will not give, receive or use any unauthorized or undocumented assistance in their group efforts as well as individual efforts. All appropriate sources need to be referenced and it’s best to do so in IEEE format for references/sources. For details on CSU academic integrity policy goes to: http://learning.colostate.edu/integrity/index.cfm

Problems will be solved according to CSU policies: http://tilt.colostate.edu/integrity/guides/what to do.cfm

I hope by the end of the required talks in 562 or even sooner, all students appreciate the old saw “to read without reflecting is like eating without digesting”. Or for the simple fools like me the shorter version “knowing the facts versus knowing the truth”. Finally in talks like music” know your song well before you start singing”

Cost “the four letter word’ plays a key role in 562. This is just an economic word for the common good. So in a cell phone application the IC power chip has a potential market of 2 billion/ year—so cost and size drives all design.

GRADING for 562 Power Electronics

Quick Overview: ALL efforts below are with a group from 1-6 people, so form a group ASAP.

1. Pop Quizzes: 24%
2. Home Works: 6 %
3. Spice labs: 10%
4. Talk # 1: 20%
5. Talk # 2 40 %

TOTAL 100 %
Extra credit up to 10%
Class participation: 10 %

Practice makes perfect
Kaizen is a Japanese word for” continual improvement and is common in manufacturing as pioneered by Toyota.

Presentation skills too can be honed through repetition, listening to talks and critique of our own talks
In class lectures go “outside the text” and material presented should be an introduction if not a solution to pop quizzes that occur every week. I provide pop quiz questions prior to lectures so you can be prepared to ask questions.

Otherwise the text is the major basis for grades in sections 1,2,3, and portions of 4 and 5. Indeed 4 and 5 are detailed in the syllabus, covering what is expected.

In a nut shell the ECE562 grading is scored as follows in 6 parts:

1. **(6% of grade) Four HW Homework assignments @1.5 pts each will comprise 6% of the grade.** See page 4 of this document for details of assignments and due dates from Chapters 2,3,4and 5. In general HW assignments are due on Tuesdays the week after they are assigned. I will email each of you to remind you of HW problem changes and due date changes if any.

   Roughly speaking, HW due dates for the HW assignments are as follows UG is undergraduate and they do only a HW problems indicated, whereas graduate students do all assigned problems:

2. **(10% of grade) Five Spice assignments @ 2 pts each are worth 10 % of the grade and are described in detail on the webpage and below I give the schedule of SPICE due dates.** In general Spice labs are due on Tuesdays too, usually when no HW is due. Use student versions of Cadence, NL5 or LT(linear technology website) SPICE ALL OF WHICH ARE FREE.

**NL5 Spice Simulator vs. Cadence Virtuoso for Spice Labs of DC to DC converters**

NL5 Spice Simulator and Cadence Virtuoso are programs that allow users to design circuits in a schematic view and then run various simulations on the designs. While they both have schematic capture and simulation capabilities, the extent of those capabilities are very different.

Cadence Virtuoso is an industry standard software package that provides full IC design, from schematic design and simulation all the way up to physical chip layout. Cadence requires detailed parts libraries in order to simulate real components sold by different vendors, which is needed when designing real life chips. The main advantage Cadence has over NL5 is its extensive capabilities. Cadence offers every type of simulation, design check, and various tools a designer would ever need in a circuit-design package, and is regularly used in large-scale chip design in the IC industry. Some of the advanced simulations Cadence offers include simulating
different design corners, Monte Carlos sweeps, and process variations. When used at its full potential, Cadence is a very powerful circuit-design program.

Cadence has two main disadvantages however, which are cost and complexity. It is a very expensive software package that typically costs companies and school thousands of dollars per license. For the most part, only large organizations can afford Cadence, so smaller companies or individuals must look elsewhere. In addition to its high cost, Cadence is also a very complicated program to master. It usually takes years just to learn to use a lot of the more common schematic simulation modes. Using layout and the more advanced simulation modes further increases the complexity of the program. In short, in order to use Cadence to its full potential and “get your money’s worth”, one must spend several years mastering the software. For students trying to use a circuits program for the purpose of learning circuit theory, Cadence is an ineffective option since it is so expensive and takes so long to learn how to use.

NL5 on the other hand is a very good candidate to use for educational purposes. To start, it is completely free to download and use. Unlike Cadence, it can be installed on Windows or Mac, and is a very small program (Cadence is typically run on Linux, and is a massive software package, memory-wise). In addition, NL5 is extremely simple to use compared to Cadence. It has a very straightforward GUI that is not overloaded with unnecessary content. The components in the somewhat limited library are all very basic and easy to assign values to. Simulations (AC, transient, and parametric sweeps) are pretty easy to master after going through a step-by-step tutorial of them. Another important point is that nearly all of NL5’s functionality is always visible and available to the user on the schematic design screen. This means that it is not necessary to search through bloated drop-down menus for different parts of the program. Because of its simplicity, NL5 is relatively easy for students to pick up and use to build basic circuits and run basic simulations for the purpose of learning how different circuits work.

While the simulation capabilities of NL5 are much lower than Cadence, it is the better choice for educational settings because of its low cost (free!) and simplicity. Using a program like NL5 allows students to spend most of their time running simulations and analyzing circuits, and not troubleshooting the program itself or trying to learn how to use basic functionality.

5 Required SPICE Assignments@ 2 points each (10 Points).
Together the five labs will lead you through the major commercial DC to DC converter circuits: Buck, Boost, buck-boost, SEPIC and Cuk.

Note below that there is EXTRA CREDIT FOR THOSE who do Spice analysis for either the L-C-C or C-L-L resonant circuits, which can be found in the course website.

3. TALK #1 20 % of final grade

(20% of grade) Talk #1/Paper #1 given as a group effort will count for 20%. Talk # 1 will tentatively occur from Tues. 22nd Sept to Thur. 1st Oct., where each of four student groups are talking for the entire class period.

Each group must sign up for a specific date and with the same topic for TALK # 1 “Trends in PWM Converters: New Switches, Multi-phase parallel topologies and Coupled Inductors Employed in Multi-Phase PWM Converters for reducing current ripple but not sacrificing transient response: theory and applications”.

To make this a learning experience and to insure “you get it” I expect you to cover the following issues for the % of the talk #1/paper grade indicated below by sub-topic for either synchronous Buck or synchronous Boost converters:

a. (15 %) Compare passive Si versus SiC diodes in conventional Buck or Boost converters with one FET switch

b. (15 %) Describe the replacement of the diode with an actively driven FET (synchronous Buck or Boost) and compare to the diode version

c. (30 %) Paralleling many Bucks or Boosts (multi-phase Buck or Boost) it is possible to achieve increased di/dt performance yet maintaining low ripple DC. Explain by circuit drawings and circuit equations how this is accomplished by:
   1. Switching all FETs in unison
   2. Phasing the FET turn on so ripple is reduced by phase cancelation
   3. Comparing the performance of a versus b above

d. (40 %) Multi-phase bucks have increased ripple currents in each stage. To decrease this we use coupled inductors with each pair of Bucks in parallel as discussed extensively in class.

Now explain by circuit drawings and circuit equations: “Coupled Inductors Employed in Multi-Phase PWM Converters for reducing current ripple but not sacrificing transient response: theory and applications”.

Let me know if your group needs a specific talk date as early as possible. Email the PPT SLIDES to me as email attachments, only after taking into account the issues raised by myself for additional effort, at your talk. Word Paper is sent to the grader ONLY, as email attachments so we have a record of receipt date versus the due date.
I strongly recommend Microsoft SkyDrive for student cooperative projects/talks/papers that many students in a group can share edits as they occur. It is deeply integrated with Microsoft Office on both Windows and Mac’s.

4. TALK #2 (40 % of grade)

In your group talk #2 be sure to cover the two legacy issues below, before you cover PWM Based LED power supplies and compatibility with legacy dimmer fixtures as well as the non-linear V-I characteristic of LED sources, which are the load for the PWM power supplies

1. Incandescent lights left behind the legacy Edison Screw that all new replacement lighting for incandescent must employ—also the wall fixture for "dimmers" is a legacy

2. Florescent lights left behind a new linear light fixture for linear florescent bulbs as well as the use of phosphors to tune the desired color spectrum of the output light—use differences of commercial florescent light phosphors for differing indoor lighting

AGAIN These legacy issues must FIRST be addressed in your talk # 2 LED lighting of spherical bulb or linear types

Then launch into DC power supplies for LED lights available commercially of both constant output V and constant output I assuming an available DC input and desired DC output

Finally for the last part of the talk take into account the LEGACY wall fixture "Dimmers" that use SCR's to chop the input grid sinusoid to vary input power. This electrical interface with the grid and must ALSO be employed to dim LED lights when one employs the legacy dimmer wall fixture—this is a big challenge as you will discover for LED dimmer capability in legacy fixtures—and places additional burdens on the PWM circuits for dimming

Talk #2/Paper #2 given as a group effort will count for 40%. Talk # 2 will occur weeks from Tues. 3"rd to Thur. 12"th Nov., with each with each of four student group talking for the entire class period. Each group must sign up for a specific date and ALL groups must cover a topic interest to the group in power electronics.

Any topic in power electronics is fine but I prefer the topic of Dc to AC converters

PART ONE OF PAPER/TALK #2: 35 %
1. DC to Ac converters for the AC Grid at 60 Hz
2. DC to Ac converters for the variable frequency motor drives

PART TWO OF TALK #2 /PAPER: 65%
b. (65% of talk/paper #2 grade this is a power electronics course after all) The
details of synthesizing AC wave forms from DC with both variable amplitude and
variable frequency
1. (20% of talk #2/paper grade) Discuss power factor requirements of the
EU’s 61000-3-2 which specifies acceptable levels of the first 32 harmonics of
the AC mains (3%).
2. (45% of talk #2/paper grade) Describe in detail the electronic interface
circuits for variable frequency motor drives using commercial examples

FALL RECESS begins 23rd Nov. till 27th Nov.

However, some students need a better 562 grade for various reasons—here is a chance to
earn it, by doing extra items 7 below.

Up to 10% of the grade will be for in class participation—you cannot act like a potted plant and
expect credit for this portion if for some personal reason you are not keen about interacting in
class—please see me to better allow for this portion of the grade to better serve you. Folks
who interrupt or bring to lectures quality questions or important comments will earn these
points. I love questions from the class. You are paying to be taught and I am being paid to
teach so ask lots of questions. Do not act like a potted plant in class.

In addition I will give up to 5 extra points on the final grade for a pre-approved special project to
improve the 562 course in future years (See me and we will write a contract together). An
example is to design converters using the TI website below to drive LED series or parallel
strings and compatible with legacy dimmer electronics.


Of course you will need to submit PDF’s of all your key screen shots to get credit.

FINAL GRADES

YES the possible total is >100% and final grades will be curved as described below:

Our approach will be more traditional with both + and - letter grades to achieve a sliding curve
and a distribution of grades. In an ideal statistical world we would seek in a class grade
distribution as follows:

Grading will be curved with students above the median receiving an “A”, students below the
median and above one standard deviation below the median receiving a “B”. 1 to 2 standard
deviations below the median will receive a “C”, 2 to 3 standard deviations below will receive a
“D”, and anything lower will receive an “F”.

With plus minus grading this becomes:

> 98 A+
>95 A
>90 A-
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> 87 B+
> 85 B
> 80 B-
> 77 C+
> 70 C-
etc to < 49 F

In summary, grading for 562 is in six parts as indicated above with opportunity for both group and individual efforts. Group efforts are encouraged in HW, Spice assignments and talks as well as associated papers. Groups of up to but not to exceed 6 students per group, are acceptable to encourage team efforts and provide the opportunity to learn team dynamics. Upon leaving CSU you will work in a company in teams—the Word and PowerPoint skills you learn in presenting technical materials in 562 will be to YOUR benefit. The practice and experience of living with the “psychodrama of technical group efforts” will also benefit you personally.

### Deadlines for Pop Quiz’s, Lab’s and Homework’s

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<td>September 8th</td>
<td>Boost Spice Lab</td>
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<td>September 15th</td>
<td>Buck Boost Spice lab</td>
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<td>HW #1 : Chapter 2 Problems 1(UG), 2(UG), 3, 4, 6</td>
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<td>September 17th</td>
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<td>Pop quiz # 3 due 18th</td>
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<td>September 22nd</td>
<td>SEPIC Spice Lab</td>
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<td>September 24th</td>
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<td>Pop Quiz #4</td>
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<td>September 29th</td>
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<td>October 1st</td>
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<td>October 6th</td>
<td>Cuk Spice Labe</td>
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<td>October 8th</td>
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<td>HW #2 : Chapter 3 Problems 8(Ug), 9, 10 (UG)</td>
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<td>October 22nd</td>
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<td>Pop Quiz #6</td>
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<td>October 29th</td>
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<td>Pop Quiz #7</td>
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</table>
- **Collins 562 LECTURES RESUME Tues. 8 Oct.**

**Pop Quiz’s, Homework’s, Lab’s and paper Doc file to be sent to Grader.**

**REVISED PPT slides from both talks 1 and 2 to me**

**Talk #1:**

**Sign up your group for one of four group talk # 1 dates between Tues. 22Sept to Thur. 1 Oct.**

All groups have the same topic:

**Talk # 2:** From Tues. 10th November to Thur. 3 Dec. are reserved for TALK # 2. Spring break is in the middle from 20-29 Nov.

- **TALK #2 (40 % of grade: 35 PPT talk and 5 WORD PAPER)**
  - PPT Presentation is grades as follows:
    1. **TECHNICAL ACCURACY** 18/25
    2. **PPT Slide ORGANIZATION** 6/25
    3. **CLARITY OF MATERIAL-SHORT LIST OF TOPICS IN DEPTH COVERAGE BETTER THAN MANY TOPICS VERY SHALLOW DOVERAGE** 2/25
    4. **PROPER SPELLING GRAMMAR REFERENCES** 2/25
    5. **FOLLOWING THE MEMOS ON TOPICS TO BE COVERED** 2/25

- **WORD PAPER GRADE OUT OF 5 AS FOLLOWS:**
  1. **TECHNICAL ACCURACY** 2/5
  2. **PAPER ORGANIZATION** 1/5
  3. **CLARITY OF MATERIAL-SHORT LIST OF TOPICS IN DEPTH COVERAGE BETTER THAN MANY TOPICS VERY SHALLOW DOVERAGE** 1/5
  4. **PROPER SPELLING GRAMMAR REFERENCES** .5/5
  5. **FOLLOWING THE MEMOS ON TOPICS TO BE COVERED** .5/5
No class **Thur. 19th November** before fall break, to make up for over runs in prior classes.

For all groups the same general topic is described in detail in the syllabus but as a crude title use "Theory and application of DC to Ac converters for both the AC grid Ac and for variable frequency motor drives".

Three student groups present for an entire class period as shown on the dates below:

- **Tues 10th November** Revised PPT slides and Word version of talk # 2 due one week later.
- **Thur. 12th November** Revised PPT slides and Word version of talk # 2 due one week later.
- **Tues. 17th November** Revised PPT slides and Word version of talk # 2 due one week later.

Fall break from 23 to 27 Nov.

**If needed the last talks are Tues1 DEC**

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<tr>
<th>DATES</th>
<th>Week #</th>
<th>Tues Due Date</th>
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<tr>
<td>1/3 Dec</td>
<td>15</td>
<td>Revised PPT slides and Word version of talk # 2 from 17 Nov. due 3 Dec</td>
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<tr>
<td>8/10 Dec</td>
<td>16</td>
<td>EMC/ EMI Lecture Tues. 9 Dec and grade estimate Thur. 10 Dec</td>
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**Special Talk # 2 opportunity for students in BOTH 461 and 562**

Motors and motor drives are key technologies for a variety of reasons. First >60% of grid energy goes to motors. Moreover, improvements in efficiency from input AC power to Torque-RPM mechanical energy at loads is an on-going green revolution as it creates "Negawatts" of saved energy that need not be generated. Electric cars will also be more competitive with these "variable frequency" motor drive improvements.

In short the goal of the new power electronics technologies is increased efficiency motor operation, smaller size and lighter weight electric motors and eliminating the need for
mechanical gear trains to meet the applications specific $T_{OUT} - N_{OUT}$ mechanical load requirements by variable frequency drive electrical means alone. 

So a special opportunity is offered to students in both 461 and 562 courses to do talk # 2 on motors/motor drives. An emphasis list of items to cover is given below for 461 presentations and a different list of items for 562 student presentations. Students MUST add to this according to their group's interests. For those students who will give the same talk in both classes both emphasis lists must be covered in the presentation that will give twice once in each class.

461 Presentations Required High Points:

1. Describe the $Z_{IN}$, $V_{IN}$ and $I_{IN}$ seen by the power electronics drives (e.g. the motor's electrical input characteristics) versus the varying $T_{OUT} - N_{OUT}$ curves of the mechanical load for:
   a. Brushless DC Motor (BDCM)
   b. Synchronous motor
   c. Permanent magnet Synchronous motor (PMSM)
   d. Induction motors

   In short review the $T_{OUT}-N_{OUT}$ vs $V_{IN}$ - $I_{IN}$ curves for the four most used motors.

2. Provide web links to manufacturers spec and application notes and their major arguments to justify the separate claims that "PMSM" technology is the best versus "BDCM" technology is best versus Synchronous or induction motors. This is easily resolved by distinguishing what mechanical loads each technology is best suited for. Do this for the four the chosen motors at the three mechanical load levels of:
   a. Low HP < 1 HP
   b. Medium HP < 10HP
   c. High HP > 100 HP

3. Commercial motor control systems consist of: sensors, command and control chips and power train drives.
   a. Describe in detail spatial location, type and output levels from the sensors for rotor position and other motor parameters needed for control decisions.
   b. Give three commercial motor control chips or board level hardware control systems.
   c. Compare and contrast the advantages and limitations as well as cost of high power switch hardware in the drive train employing:
      a. Thyristors
      b. IGBT’s
      c. IGCT’s and it’s variants of MOS control

   Go to manufacturer’s websites and get specs for the high power switches as well as application sheets for motor drive applications with these same switches and their control drive electronics.

d. Provide two examples of commercial power train electronics from switch drives to variable 3 phase output $V(f)$ from power switches.
562 Presentations Required High Points:

1. Explain the cost and reliability considerations for the motor centric items listed in 461 point #1 as well as the best of the breed for applications at the three HP levels for the four motor varieties:
   a. Brushless DC Motor (BDCM)
   b. Synchronous motor
   c. Permanent magnet Synchronous motor (PMSM)
   d. Induction motors

2. Explain in detail the differences and advantages as well as disadvantages of DSP vs FPGA vs microprocessor control methodologies and switch algorithm flexibility as well as cost.

3. Discuss the R-L-C components both within and external to motors as regards their maximum operating voltages, currents and frequencies.

Again if the same talk is given in both classes all of both high points at minimum must be covered as well as the student group's own topics.

Thank you again for reading though this 13 page missive. If you have further questions ask me in class so everybody benefits.

Instructors Teaching philosophy

ECE Students are the most important people at CSU.
Not dependent on faculty.
Faculty is dependent on them.
Not an interruption of our work.
They are the purpose of being at CSU.
Students are doing us a favor when they come to our office.
We are not doing them a favor by serving them.
Students are part of our business, not outsiders.
Not just a CSU ID number.
They are flesh and blood human beings with feelings and emotions.
Students come to us with their needs and wants.
it is our job to address them with courteous and attentive treatment.
Students are the life blood of this and every university.
Without them we would close our doors.
DON'T EVER FORGET THIS