Lecture 37

Introducing Discontinuous Conduction Mode

A. Discontinuous Conduction Mode (DCM) versus Continuous Conduction Mode (CCM): Circuit Topology Transitions

1. Review of CCM and Transition to DCM
   a. Buck and Boost Examples
2. Unidirectional Current Flow Switches: Simple Diode
3. Ripple on Switch Mode Signals Versus DC Levels
4. Bi-directional Switch Insures CCM Operation
5. Summary of DCM Conditions

B. Empirical Differences in CCM versus DCM Operation

1. System Dynamics and AC Transfer Functions
2. Equilibrium or DC Transfer Function Changes
   a. Buck
   b. Buck-Boost

C. Quantifying the CCM to DCM Transition

1. "K Parameters": $K_{critical}$ versus K Plots
   a. General Concept of $\Delta I > I(DC)$
   b. Buck Case
   c. Boost Case
   d. Buck-Boost Case
2. I(critical),$R_{critical}$ and $K_{critical}$ and their comparision with K(D)

Lecture 37

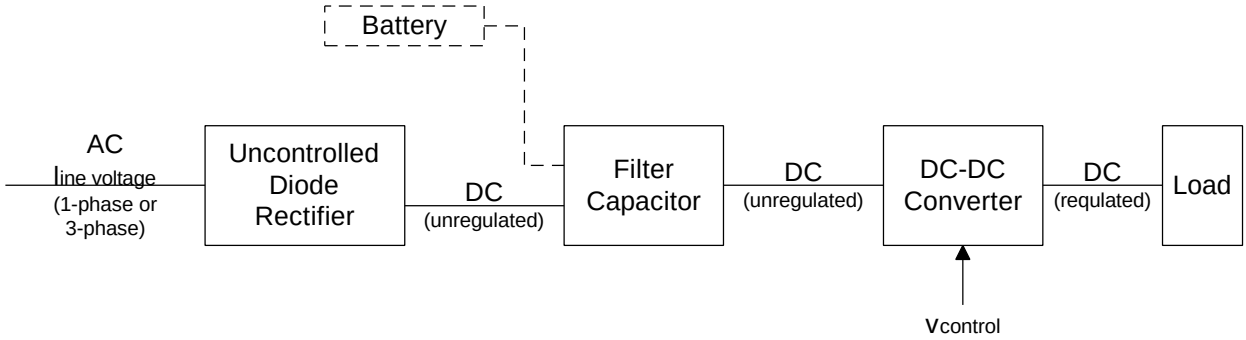
Discontinuous Conduction Mode

A. Discontinuous Conduction Mode (DCM) versus Continuous Conduction Mode (CCM): Transitions

1. Review of CCM and Transition to DCM

We show below an UPS converter block diagram to review the basic blocks of a PWM or switch mode converter.

1. UPS (Uninteruptable Power Supply) Converter Block



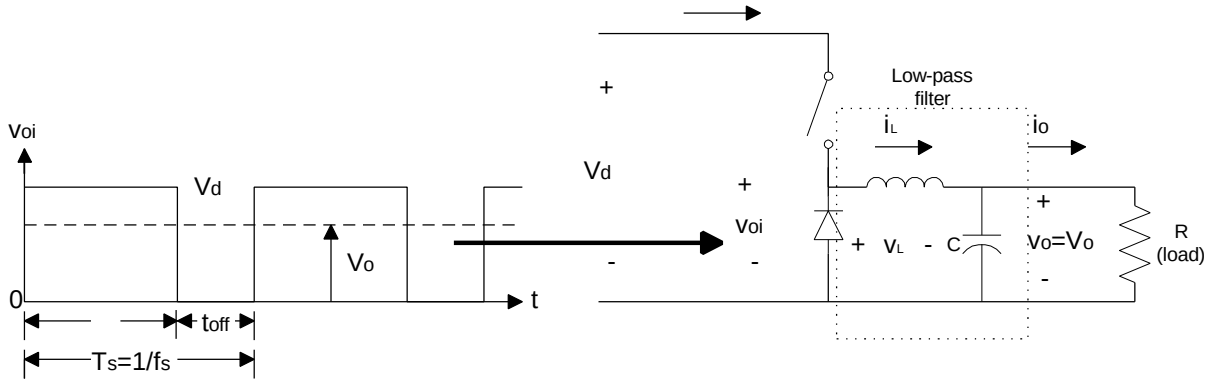
Mains — Low EMI Rectifier — Feedback — Highly Stable DC output

Consider a converter with operation in a <u>single quadrant</u> of V_o - I_o operation at the load. The 50-60 Hz mains is converted to DC. The DC acts as a voltage rail for square wave generation at the switch frequency, which is 10^3 to 10^4 larger than the mains value. The key to achieving a stable DC output, from the switch mode signal is two-fold. One is the use of an output filter set at near the switch frequency and two the use of feedback to alter the duty cycle of the switches to achieve a controlled DC output.

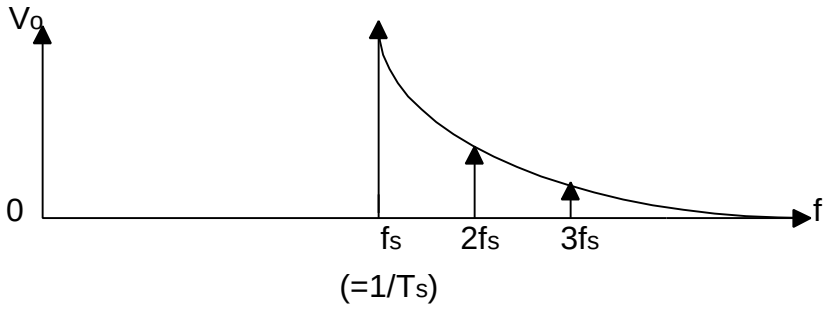
We need to make a careful choice of L and C low pass filter

elements at the load to achieve low ripple dc output.

PWM Signal Input to LC Filter



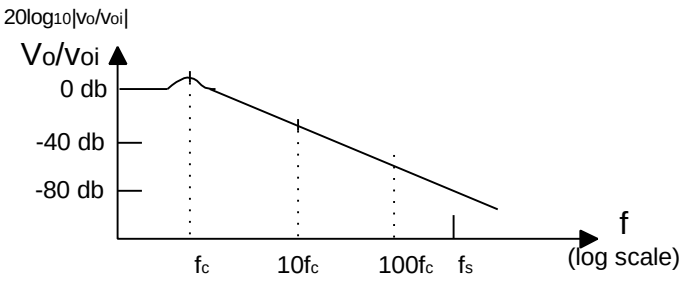
The frequency spectrum for a square wave of peak value V_{oi} has a simple Fourier spectrum as shown below in terms of the switching frequency f_{sw}. We showed previously the Fourier coefficients of the square wave vary as $(2V_{oi}/n\pi)Sin(n\pi/2)$. We must set the low pass filter to attenuate heavily all signals with $f > f_{sw}$.



Usually simple two pole filtering f_c of a single L-C section allows for a 40 dB/decade drop in signal above the cut-off frequency.

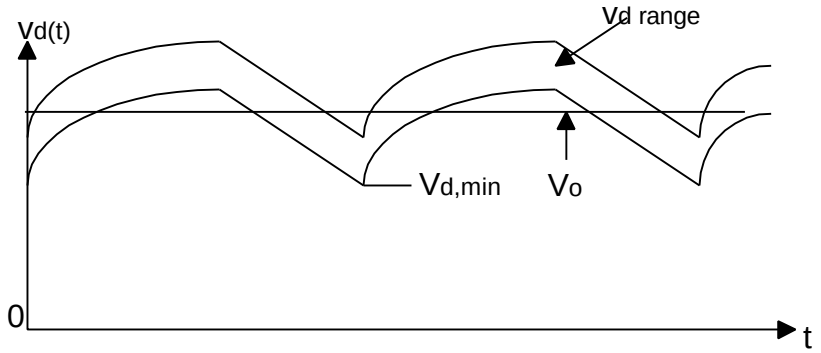
$$f_c = \frac{1}{2p\sqrt{LC}}$$

What we will see in CCM to DCM transitions is that the AC signal into the L-C filter will change wave-shape. Hence, the output DC level is expected to change when this occurs.



$\frac{V_o}{V_{oi}}$ is flat or DC-like below f_c and rolls off at 40 dB / decade above f_c. Placement of f_c compared to f_{sw} is one key decision to be made by the PWM dc-dc converter designer.

After the output filter you have an effective DC $V_o = M(D)V_{in}$ plus the ac ripple. Whose magnitude is set by the filter design. So for a variation of $V_{oi} = V_d$ level we will see at the output a ripple variation in normal CCM operation.



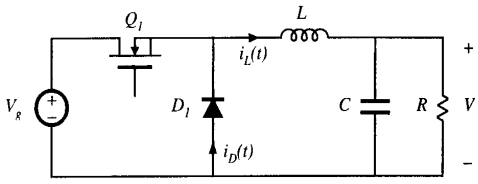
As we will soon see it is the relative value of the AC ripple,ΔI, compared to the dc levels, I(DC), that is crucial to the transition in circuit conditions from the CCM to the DCM. Usually this occurs at light loads where $\Delta V(ac) > V_{DC}$. Since all switch mode power supplies can be operated open circuit or at light load we have to deal with DCM in a complete power supply design. We cannot avoid DCM of operation.

2. Review of CCM and Transition to DCM

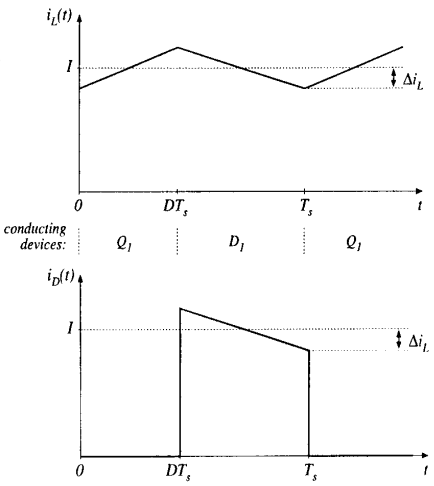
a. Buck and Boost With Unipolar Switches

1. Buck Circuit

Buck converter example, with single-quadrant switches



continuous conduction mode (CCM)



Minimum diode current is $(I - \Delta i_L)$

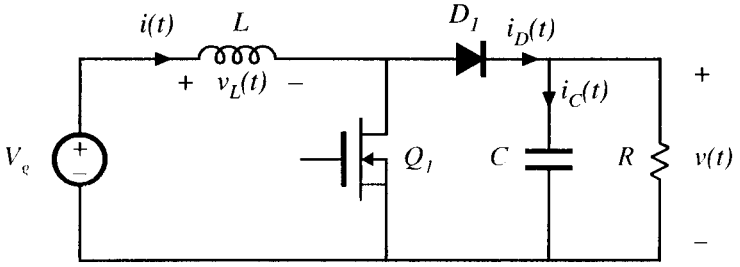
Dc component $I = V/R$

Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

2. Boost Circuit



Mode boundary:

$I > \Delta i_L$ *for CCM*

$I < \Delta i_L$ *for DCM*

Previous CCM soln:

$$I = \frac{V_g}{D'^2 R} \qquad \Delta i_L = \frac{V_g}{2L} DT_s$$

3. Brief Introduction to DCM operation

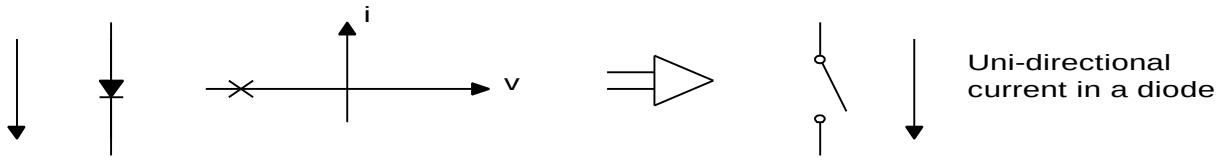
Since both ΔI and I vary with circuit (L,R,Vg)and timing parameters, D, we can set a condition for ΔI> I. In CCM the transistor and diode alternatively conduct and the switching period T_s has only two portions: DT_s (transistor-on and

diode-off) and D'T_s (diode-on and transistor-off). We thus have two electrical circuits occurring over a switch period.

In PWM dc-dc converters we can find load conditions where circuit voltages and currents are zero for a brief time interval. During this unique interval, **a new and third circuit topology combination not normally allowed is now possible. This is** called the DCM mode and will turn out to be a big practical advantage in several ways. In the DCM mode the DT_s interval is usually unchanged because the transistor conduction is controlled solely by the control signal D, which is independent of circuit operation. However, the **D'T_s period is divided by circuit conditions into two new portions, often called D_2, and D_3. T**he diode conduction duration depends solely on the circuit conditions which change during the D'T_s interval to shut –off the diode prematurely. When turn-off occurs depends on the load conditions. The value of D_2 or D_3 in DCM operation becomes an additional unknown in addition to D. This division of the D' interval into D_2 and a new D_3 interval usually happens when I(out) has a minimum DC value called the critical current, $I_{critical}$. DCM usually occurs at light load and V_{out} jumps up from its CCM value**, for the buck-boost** converter, to a higher value output-voltage as we will see herein. This can be very useful for power supplies employed for starting fluorescent lights, which initially have zero load till gas ignition or breakdown occurs. That is we need an initial large voltage to start the lamp. It could be deleterious for a microprocessor or logic power supply if the over-voltage damages circuits.

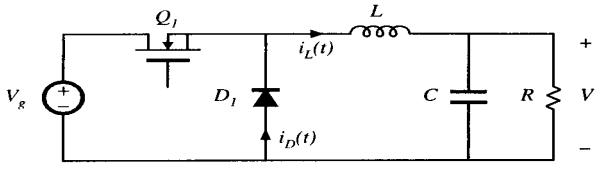
2. Unidirectional Current Restriction of Solid State Switches will insure DCM of operation.

Consider a simple uni-directional current flow diode:



The switch mode circuit conditions alone make the diode to switch on/off **in synch with the actively driven transistor**. We need no active diode control. However, in some cases shown below the diode is inadvertently shut off when I(load) < I_{DC}(min), regardless of the transistor switch state. This introduces a third circuit condition or state within the switch period, to the two states we have considered so far in CCm operation. This third state will alter both average DC and AC properties of the basic converter circuits. Lets look at the Boost circuit as we reduce the DC current level at the load. We still have the case above that the inductor current is positive and flows through the diode during the entire switch period. However, this is precariously depending on the DC level of the inductor current. What occurs if we reduce the DC current level lower than that shown above?? Can the diode conduct a negative current? What does the negative current do the inductor current waveform. In turn does this create a third circuit condition that we have been droning on about? Lets do this in two steps. First at the edge---

Increase R, until $I = \Delta i_L$

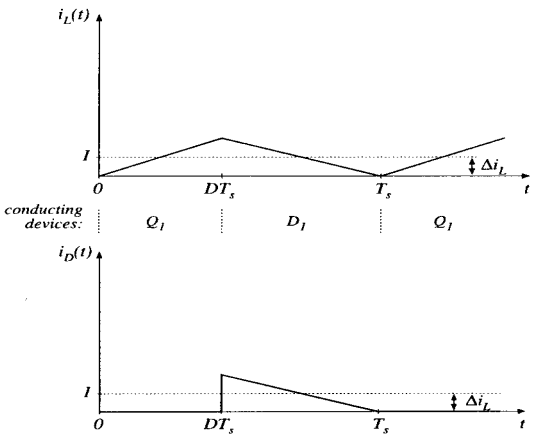


Minimum diode current is $(I - \Delta i_L)$
Dc component $I = V/R$
Current ripple is

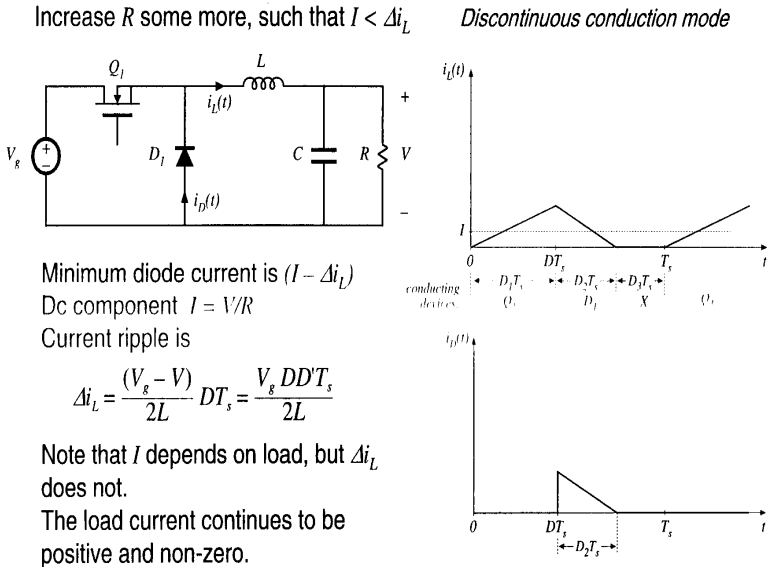
$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

CCM-DCM boundary



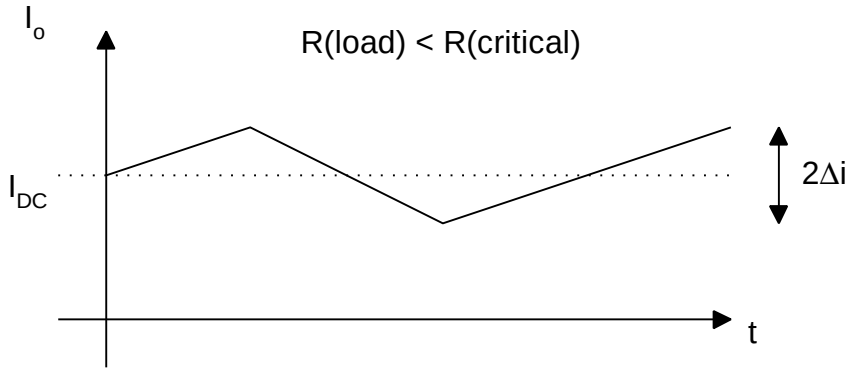
Now over a portion of the switch period the inductor current



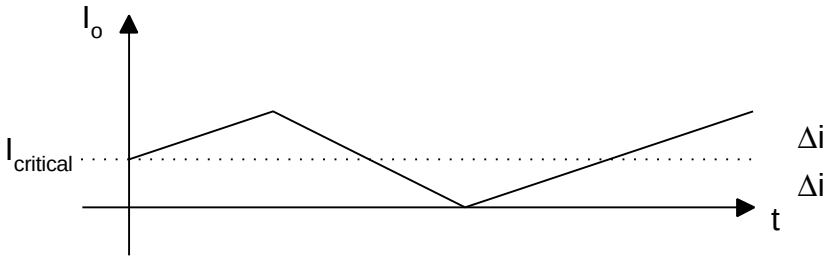
is zero and the diode is turned off creating a third circuit condition. One can think of this transition, from two circuit states per switch period to three circuit states per switch period, as the CCM to DCM transition. Let's do this another way, by concentrating on the value of the AC ripple.

3. Large Ripple Compared to DC levels occurs for all PWM DC-DC converters at low load current.

Usually the AC ripple level is fixed by the output L-C filter design. We will see later that we can have a critical capacitance value that makes the ripple too large and causes CCM to DCM transitions. As I_{DC}(out) reduces at light load the ac ripple eventually exceeds the dc levels. This is shown below.



For large I_{DC} the current is always positive, never going negative. This case is insured by a low load resistance, that draws a high DC current. Given the size of the ripple, there will be a load resistor where I_{DC} decreases to a critical level. If $R > R_{critical}$ then I(load) will decrease but the Δi remains the same. Eventually, Δi will TRY TO GO NEGATIVE, but the diode will not allow this polarity current flow to occur. Below we show I(load) just reaching I(critical). I(critical) will separate the CCM and DCM operating modes.



CCM case $I_{critical} \geq \Delta i$; $I_{critical} \leq \Delta i$ DCM occurs

Since Δi in the converter circuit usually varies as V/L we can also state that DCM occurs when the circuit inductor is too small. L must be large enough to maintain Δi small enough at $I_{out} < I(critical)$. Otherwise the diode cuts off and we get a third Circuit State during the switch period.

CCM	DCM
$V_o \neq f(R_L)$ Ideal	$V_o = f(R_L)$ Non-ideal
$V_o/V_{in} = M(D)$	$V_o/V_{in} = M(D, R_L)$
V_o/V_{in} steady at light load	V_o/V_{in} jumps up at light load

Boundary

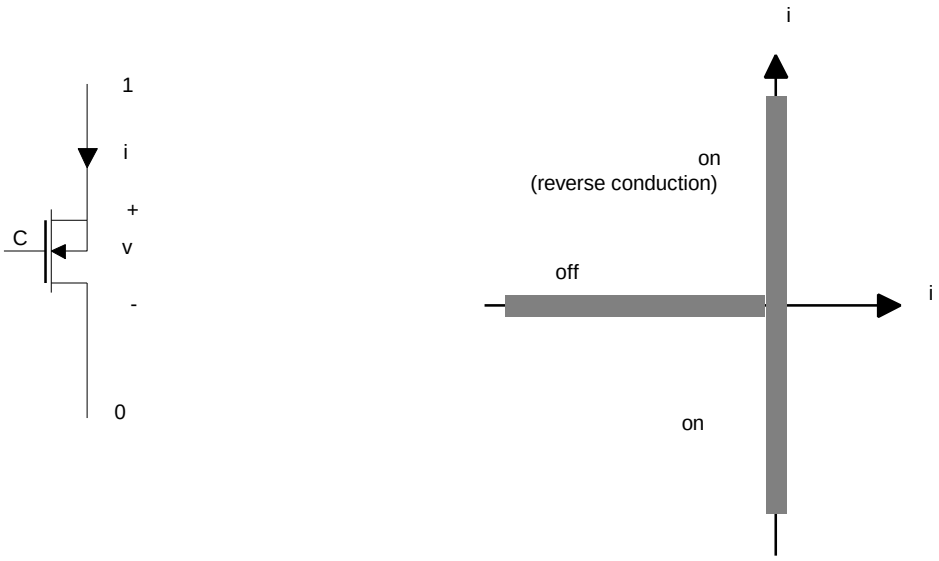
$I_{AV}(out) > \Delta i$ $\quad$ $I_{AV}(out) = \Delta i$ $\quad$ $I_{AV}(out) < \Delta i$

$|\Delta i| = I_{critical}$

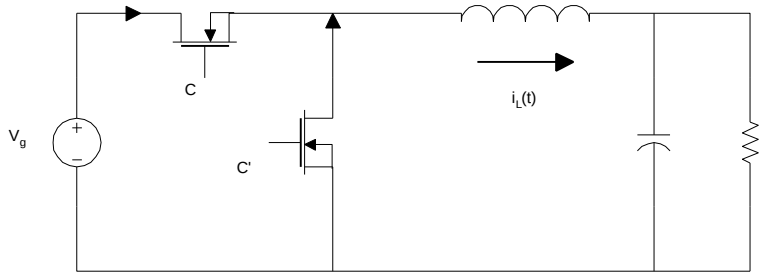
CCM	DCM
Ideal V source	V source with $V_o = f(R_L)$

4. Bi-directional Switch to Insure CCM Operation

For the same converter topology a different choice of solid state switch other than a diode means the same converter can NEVER operate DCM. The simplest case occurs when we replace the unidirectional diode with a power bi-directional MOSFET in the buck converter. Of course in this case the bipolar series transistor and the shunt CMOS transistor have complementary switch drives C and $\overline{C}$. Notice that the MOSFET must be inserted into the circuit with source and drain connections reversed, to replace the diode. The normal operation for the MOSFET only allows for the blocking of positive voltage but with this reversal we can now block negative voltage as well!



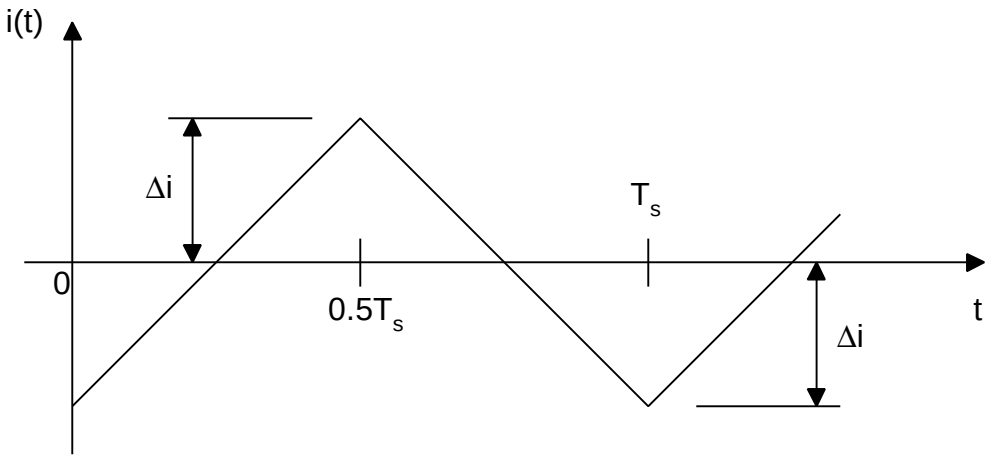
Lets consider a simple Buck converter with complementary control signals to the two switches as shown below:



Buck converter, implemented using a synchronous MOS rectifier. Can this circuit with a MOS transistor replacing the

diode ever operate DCM? No, this converter cannot operate in DCM because the “synchronous rectifier” is a “two-quadrant current-bi-directional switch.” Thus, a change in current direction, positive or negative, will not turn the MOSFET off. DCM occurs when the switches are unipolar BUT V or I is bipolar. This always occurs when the output is unloaded for all converters.

What if $R \rightarrow \infty$? (open load)--will we still get CCM operation using a MOS rectifier?



For $R \rightarrow \infty$, the “dc component” of the current becomes zero. The ripple remains, and causes the current to be positive for half of the switching period, and negative for the other half. The CMOS transistor can handle this in the CCM. Contrast this behavior to the diode behavior, which goes on/off as set by circuit voltages but not the applied control signals. The circuit waveforms alone set when we have an open or short for a diode.

Diode: on Diode: off

For gated switch devices the control signal alone sets on/off conditions and we will usually get only the two circuit conditions. However, the use of diodes in converter circuits can ensure DCM operation if we wish it to occur at low loading conditions. Let's emphasize that DCM operation is not worse or better than CCM operation. Detailed advantages and disadvantages will be given later. Some potential advantages to DCM are: automatic reset of inductor current to zero each switch cycle insuring no core saturation and the more stable AC response of the DCM of operation that we will study in Chapter 10. Please read the first half of Chapter 10 in Erickson at this time along with all of Chapter Five.

So, in simple diode-transistor switch implementation, if the load resistor is made too big (unloaded output)

$$\frac{V_o}{R} < \Delta i$$

$\Rightarrow$DCM occurs with <u>three</u> time periods within the switching interval T_s because the diode goes off when it should be on we get a third time interval D_3T_s or $D"T_s$.

We compare CCM and DCM operations below:

Heavy load	Light load
CCM operation for Buck	DCM operation for Buck

5.Summary Of DCM Operation

There are four points to be made for DCM Operation

DCM of Operation

- Occurs because switching ripple in inductor current or capacitor voltage causes polarity of applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch are violated.
- Commonly occurs in dc-dc converters and rectifiers, having single-quadrant switches. May also occur in converters having two-quadrant switches.
- Typical example: dc-dc converter operating at light load (small load current). Sometimes, dc-dc converters and rectifiers are purposely designed to operate in DCM at all loads.
- Properties of converters change radically when DCM is entered:

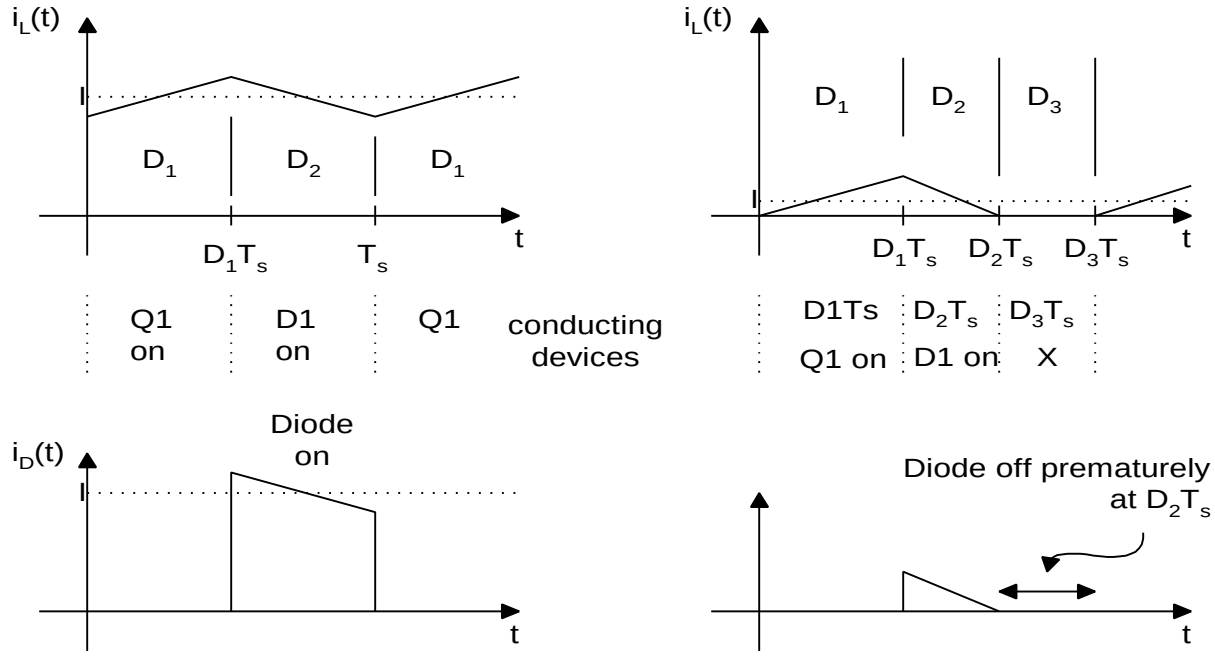
  M becomes load-dependent

  Output impedance is increased

  Dynamics are altered

  Control of output voltage may be lost when load is removed

What effect does DCM vs. CCM operation have on the circuit
conditions?



B. Empirical Differences in CCM versus DCM Operation

1. System Dynamics and AC Transfer Functions

We will see in Erickson Chapters 9 and 10 the dynamic loop gain A_{OL} is different for DCM and CCM:

CCM	DCM
a. A_{OL} has two poles-- potentially unstable to oscillation if feedback is applied.	a. A_{OL} has one pole-- unconditionally stable to oscillation with feedback applied.
b. Also has right half plane zero which enhances instability due to extra phase. This zero cannot be canceled out by a LHP pole.	b. No right half plane zeros occur enhancing stability.
c. Lower I_{peak} and V_{peak} for switch stress which means less expensive switches.	c. Higher I_{peak}, V_{peak} to stress switches which means more costly switches.

3. Efficiency of P_o/P_{in}

CCM	DCM
Higher Efficiency	Lower Efficiency

4. Z_{out} Values

CCM	DCM
Lower Z_{out}	Higher Z_{out}

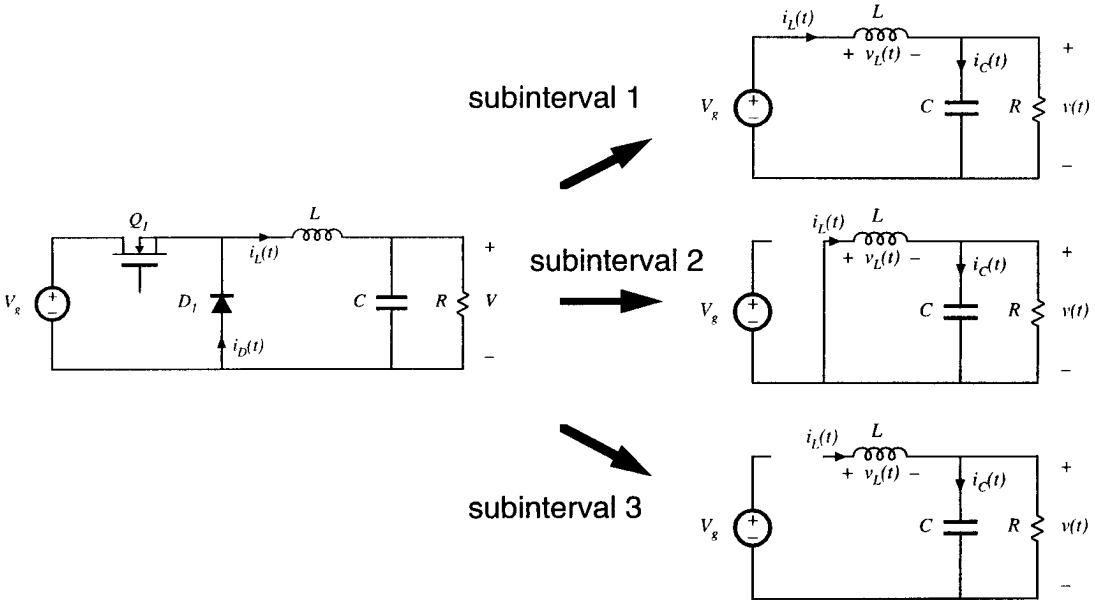
Some applications are better served by CCM or DCM operation. In short both DC and AC requirements of a given source must be well know before you choose CCM over DCM operation.

2. Equilibrium or DC Transfer Function Changes

a. Buck

The volt-sec balance across an inductor and the current – sec balance across a capacitor allowed us to determine the

equilibrium transfer functions. Now we have a third circuit to include in the balance equations over the switch period as shown below. That is, we explicitly break out the three circuit topologies that the DCM of operation brings to the party. Because there are three circuits and three time intervals, this complicates the volt-sec and A-sec balance conditions we must evoke in order to find the DC transfer functions. We also expect these transfer functions to be DIFFERENT from CCM values.



The DC transfer functions will clearly be different. Below on page 16 we outline the general case. In part b we examine the buck-boost circuit, for a specific insight into the changes the CCM to DCM transitions bring to the DC output. Finally in lecture 38 we revisit this transition for all three basic circuits and derive general solutions for the DCM transfer functions in equilibrium via the solution of quadratic equations evolving from both volt-sec and A-sec balance.

For steady state:

CCM	DCM
D_1 and D_2 only for circuit	D_1, D_2 and D_3 where D_2 is set by

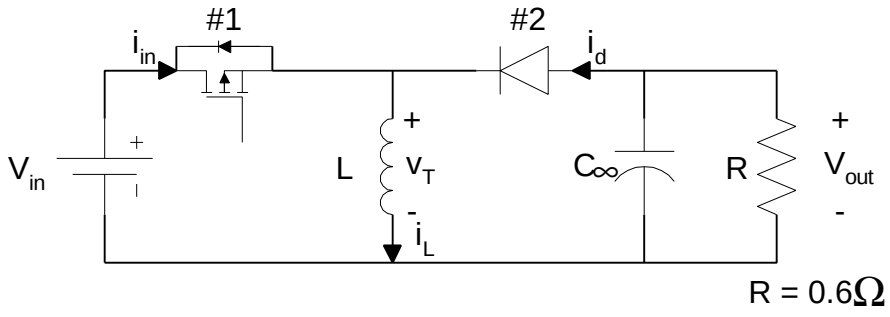
The steady-state conditions:

$\langle v_L \rangle = 0$ Two terms: D_1 & D_2	$\langle v_L \rangle = 0$ Three terms: D_1, D_2 & D_3
$\langle i_c \rangle = 0$	$\langle i_c \rangle = 0$
$\frac{Vo}{Vg} = M(D)$	$\frac{Vo}{Vg} = M(R_L, D)$
No effect on load resistance	Explicit R_L dependence

Particulars for the buck converter DCM DC transfer function will be given in lecture 38. For now realize that the transfer function is different. This means upon the CCM to DCM transition the output voltage will change. We will illustrate this below for the buck-boost where upon CCM to DCM transition the output voltage INCREASES.

b. Buck-Boost CCM to DCM Transition

Consider the buck-boost converter circuit below with C considered ∞ and L set by the designer and f_{sw} = 100 kHz, T_s = 10 μs. We will solve this first intuitively and later use a more formal approach in lecture 38.



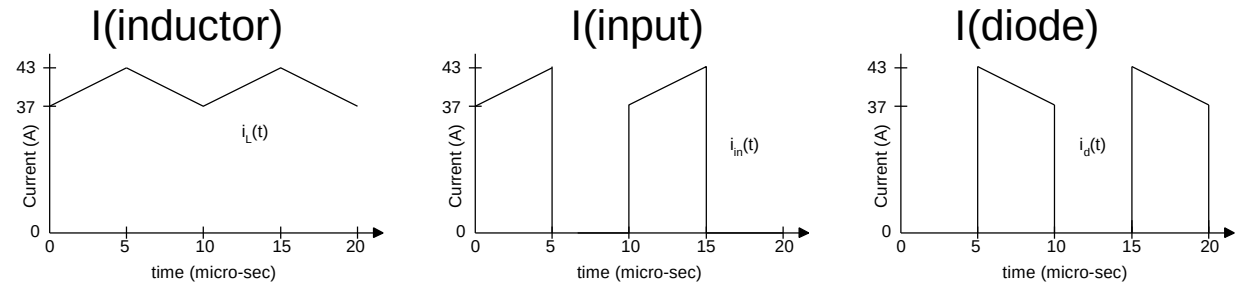
Clearly in CCM operation in steady state: $DV_{in}/D' = Vout$ yields D = 0.5 to achieve for this case the as stated conditions V_{out} = -12V with $V_{in} = V_g$ = 12V. We also know $R_{out} = 0.6\Omega$,so I_{out} = 20A. Next $I_{in} = DI_{out}/D'$ gives I_{in} = 20A for CCM operation. As we saw previously for the buck-boost the inductor current $I_2 = I_{in} + I_{out}$ = 40A. The ac conditions will be approximated by linear ramps and set by the choice of L.

What happens if R_{out} increases or decreases in the two separate cases of CCM and DCM?? **The surprise will be for DCM as we will see.**

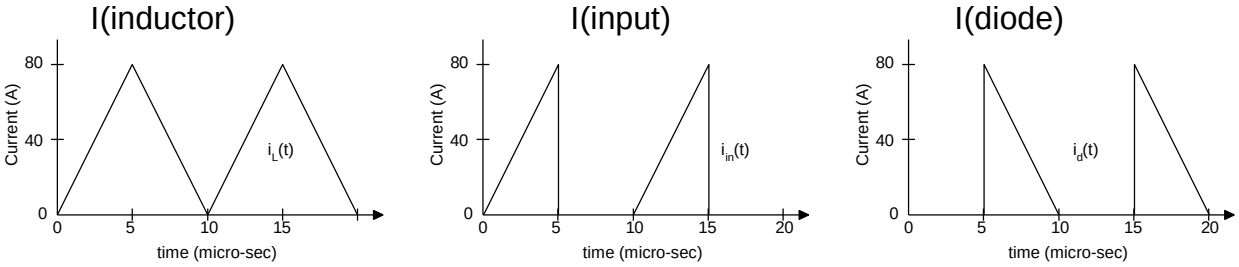
For the inductor current: $\Delta i_L = (V_L/L)dt$
At 100kHz and D=0.5 we find: $\Delta i_L = (12/L)(1/2)(10\ \mu s)$
Di_L varies with the L choice as shown below. For the first two choices (10 and 0.75 μH) CCM operation is maintained since L is big enough to keep ΔI small but for the third choice L = 0.5 μH DCM operation occurs because L gets too small and ΔI too big.

L	Δi_L	Comment
10 μH I_L(inductor) =40A I_{in}(DC) =20A	6A	CCM small fraction of 40 A = I_L(DC) I_{peak} = 43A = I_L(DC) + ½ Δi_L I(min) =37Amperes
0.75 μH I_L(inductor) =40A I_{in}(DC) =20A	80A	CCM Ripple exceeds 40 A = I_L(DC) I_{peak} = 80A = I_L(DC) + ½ Δi_L Imin) =o Amperes

These two L choices cause i_L, i_{in} and i(diode) waveforms to vary as shown below for the choice of L =10 μHenries:

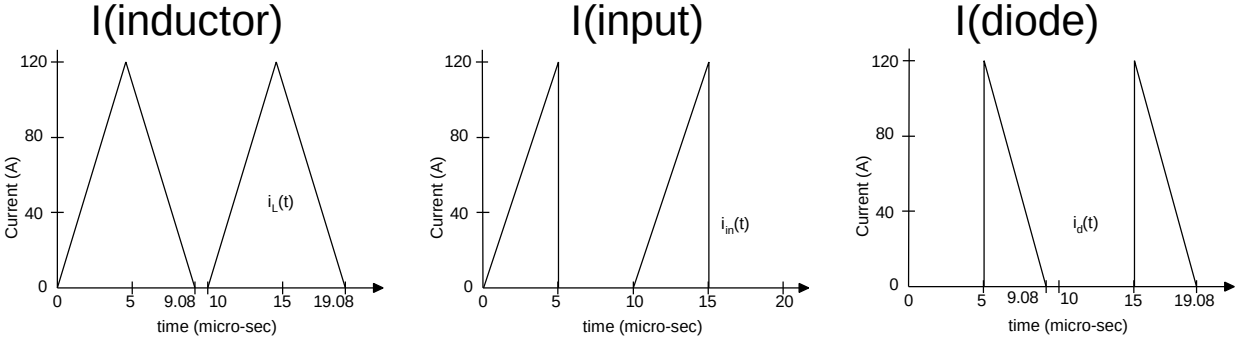


Current waveforms with L = 0.75 mH.



Current waveforms with L = 0.75 μH.

Note L = 0.75 μH is the critical inductance for it allows i_L to just reach zero at t = 10 μs. While i_{in} and i(diode) when added together just form the i_L triangle wave out of two sawtooth waves. Finally, note if R_L varies from 0.6 to 0.5Ω or lower values (but not up to 0.7Ω) there will be NO effect on the Vout for CCM operation via V_o/V_{in} is only M(D) = D' for boost. **Why is the higher resistor going to be an issue?** The third L choice, 0.5 μH, causes the i_L, i_{in} and i(diode) waveforms to vary as shown below and DCM operation to occur because the ripple is greater than the DC values. This changes the DC transfer function.



Current waveforms with L = 0.5 mH.

Assuming the active duty cycle control D = ½ is maintained on the transistor on-time we can now determine DCM current levels and compare to the prior CCM cases: Δi_L = (12 / 0.5μH) 5μs = 120A peak. In the middle curve above the average I_{in} is then given by $0.5Li^2/T_s$ = 30A, 10A higher than in the CCM case. Indeed circuit conditions are different. Let's determine quantitatively the differences.

We now have I_L(DC) = 60A , which is still twice the average I_{in} for DCM ,not the 40A=I_L for the previous two cases, so I(load) is increased by 10A from 20 to 30A. This is now consistent with $I_L = I_{in} + I_{out}$. $P_{in} = P_{out}$ also checks. What about V_{out} however is it really still -12 volts? That is for the DCM of operation, $V_o/V_{in} \neq D'V_g$ Hence, the value of -12 for the output we got previously assuming CCM operation is probably invalid.

Assuming as a starter V_{out} doesn't change (we will see this assumption is wrong) then i_L ramps down to zero in the diode-on Tr-off period we guess. L = 0.5 μH will cause i_L, i_{in} and i(diode) waveforms as shown previously and DCM operation occurs. **This will make V_o change from -12V to -14.7V as we will soon see**. Lets use power balance to try and find V_{out} assuming D remains ½ and $V_{in} = V_g$ = 12V for starters. For the transistor on-time:

Δi_L = (12 / 0.5μH) 5μs = 120A peak

This corresponds to I_{in}(average) from the i_{in}(t) plot of 30A = ½*5*120. P_{in}(average) = 12*30 = 360 W = P_{out}. This **clearly implies since R_{out} is 0.6Ω:**

V^2_{out}/R_{out} = 360 Þ V_{out} = -14.7V and not the prior value. Volt-sec balance on the inductor then yields:

$V_{in}D_1 + D_2V_{out} = 0$

V_{in} = 12V, D_1 = ½ and V_{out} = -14.7V implies D_2 in DCM operation is less than the ½ value from CCM operation. D_2 = 0.408 and D_2T_s = 40.8 μs. The D_2 value changes roughly from 0.5 to 0.4. That means the load current drives

i_L to zero before we reach 10 μs and the diode clamp holds it there until the next control pulse at t = 10 μs when i_L ramps up. We repeat the result that for the DCM of operation V_o = -14.7V larger than -12V expected from the M(D) equations alone which only apply to the CCM conditions.

For **HW#2** show if R(load) is changed from 0.6Ω to 5Ω in the DCM of operation ,then V_{out} changes to -13.4V. V_{out} is now load dependent for DCM. This was not the case for CCM of operation. Explain why.

C. Quantifying the CCM to DCM Transition

1. "K Parameters": $K_{critical}$ versus K Plots

Simply speaking we will turn the ΔI> I(DC) criterion into a more general "K parameter" derived from I and a value of $K_{critical}(D)$ derived from Δi. **K will always be $K = 2L/RT_s$ and will vary depending on the choices of circuit values and the choice of f_{sw}.** The k(critical) parameter will vary with the converter duty cycle,D, as shown below. We will compare a fixed K to K(critical) over a range of duty cycles to separate DCM from CCM operation. In general, CCM to DCM transitions will occur at some specific duty cycle and one mode of operation will occur over a specific range of duty cycles.

a. General Concept

We will show the following in this lecture that each $K_{critical}$ is unique to that circuit topology and duty cycle:

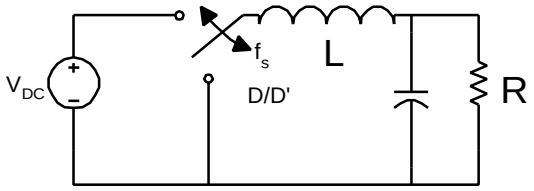
$K_c(buck) = 1 - D = D'$

$K_c(boost) = D(D')^2$ $\Longrightarrow$ employed for each topology of converter.

$K_c(buck\text{-}boost) = D'^2$

Again K will depend only on the circuit elements and the switch frequency. Now lets examine the three major converters buck, boost, and buck-boost one by one.

b. Buck Case

Buck 

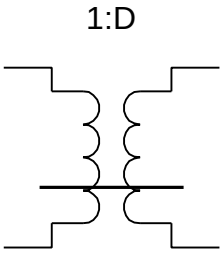
$$K \equiv \frac{2L}{T_s}\,\frac{1}{R}$$

↓

This is fixed by the circuit and switch frequency

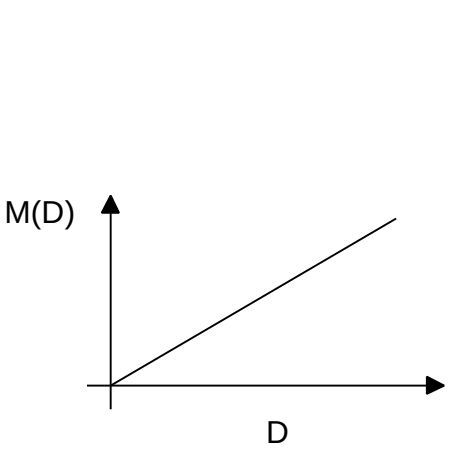
k(critical) = (1 - D) = D' and we can derive a critical load resistance $R_c = 2L/(1 - D)T_s$.

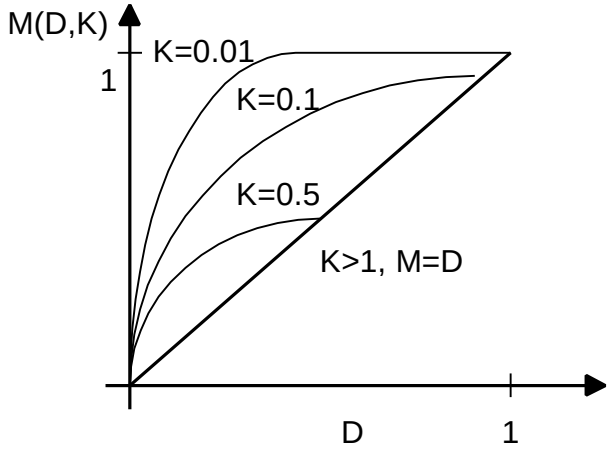
DC transformer equivalent for CCM of operation:



$$\frac{V_o}{V_{in}} = D$$

CCM Case	DCM Case
We showed previously	We will show





Note that the DC transfer function for DCM lies above CCM values at the same D value. We will prove this in lecture 38.

We are following a procedure that is really simple to set the inequalities between K and $K_{critical}$.

$$I > \Delta i_L \quad for\ CCM$$
$$I < \Delta i_L \quad for\ DCM$$

Insert buck converter expressions for I and Δi_L :

$$\frac{DV_g}{R} < \frac{DD'T_sV_g}{2L}$$

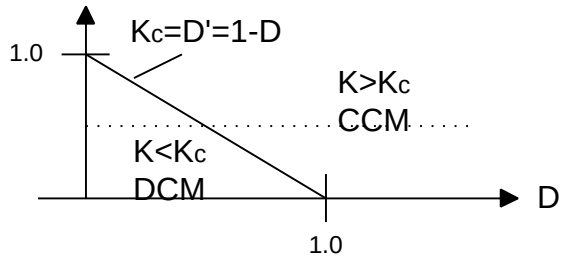
Simplify:

$$\frac{2L}{RT_s} < D'$$

This expression is of the form

$$K < K_{crit}(D) \quad for\ DCM$$
$$\text{where} \quad K = \frac{2L}{RT_s} \quad and \quad K_{crit}(D) = D'$$

Consider just the buck case below. For the k value drawn, there will be a value of on time duty cycle D that separates DCM from CCM.

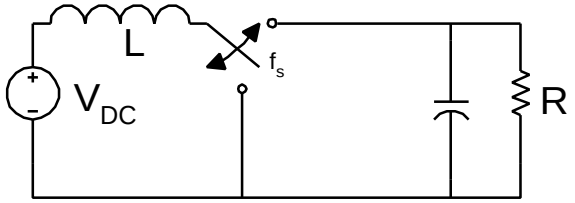


Note also that if we choose circuit parameters and switch frequency carefully K > 1.0 **we will never get DCM operation** regardless of any D employed due to K_c = D' and it will always be below unity.

c. Boost Case

Again $K = 2L/RT_s$ is chosen by the circuit values and f_{sw} choice, whereas $K_{critical}$ varies with the duty cycle in a unique way for the boost.

$$K_c = D(1-D)^2 \quad R_c = \frac{2L}{D(1-D)^2 T_s}$$



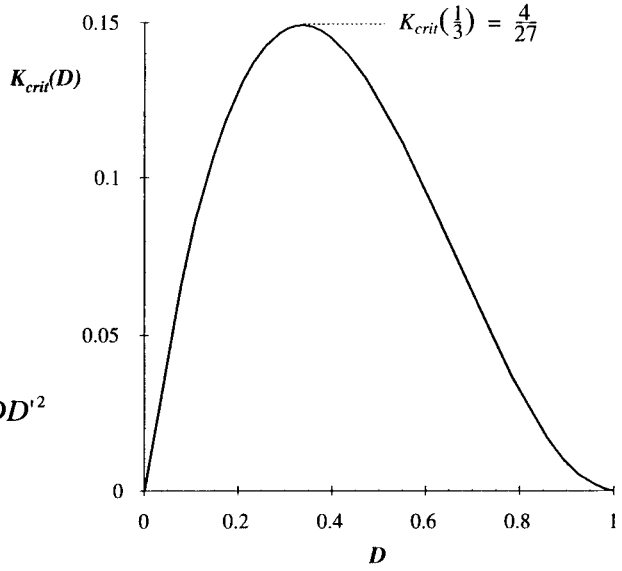
$$K = \frac{2L}{T_s}\frac{1}{R}$$

K(critical) = $D(1-D)^2 = DD'^2$ This is a function that has a maximum value K(max) = 4/27 at intermediate D values. In this case can we ever avoid DCM of operation???

$$\frac{V_g}{D'^2 R} > \frac{DT_s V_g}{2L} \quad \text{for CCM}$$

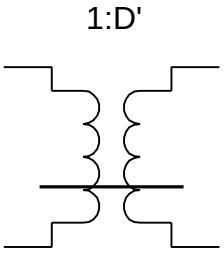
$$\frac{2L}{RT_s} > DD'^2 \quad \text{for CCM}$$

$$K > K_{crit}(D) \quad \text{for CCM}$$
$$K < K_{crit}(D) \quad \text{for DCM}$$
$$\text{where} \quad K = \frac{2L}{RT_s} \quad \text{and} \quad K_{crit}(D) = DD'^2$$



The flow of thought from ΔI> I to $K_{critical}$ plots goes as shown

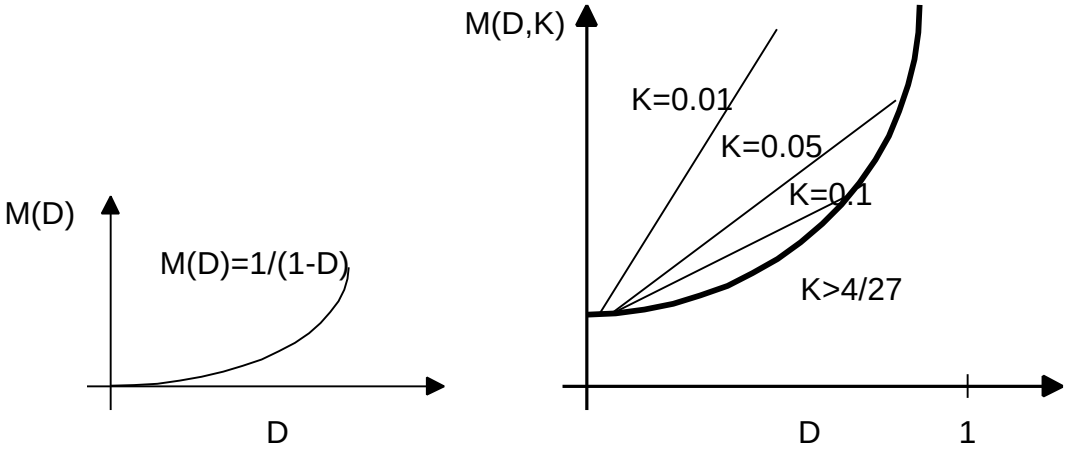
DC transformer equivalent for the CCM mode of operation:



$$\frac{V_o}{V_{in}} = \frac{1}{D'}$$

CCM Case
We showed
previously

DCM Case
WE WILL SHOW



CCM case DCM case

The CCM to DCM border occurs at a value of K(critical) dependent only on D in a quadratic manner. We choose circuit values and f_{sw} to set D to where the CCM to DCM transition occurs. Also the DCM transfer function always exceeds the CCM values for a given D value. Now $R < R_{min}$ is equivalent to $K > K(critical)$ where the CCM to DCM transition occurs.

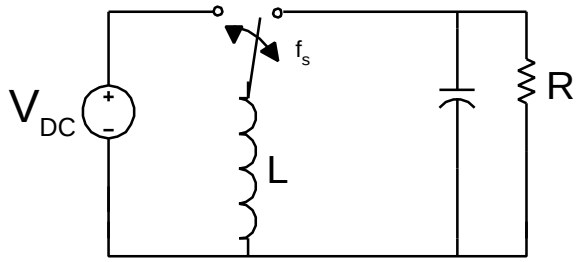
For **HW#2** prove that $K_{critical}(max)$ is only 4/27 so that k can be chosen by circuit value choices so that DCM never occurs, if desired. What happens if $K < K_c$? Are there

ranges of D that provide DCM and CCM? Be specific.

d. Buck-Boost

$$K_c = (1-D)^2 \quad R_c = \frac{2L}{(1-D)^2 T_S}$$

Again K is set by $2L/T_s$ circuit and f_{sw} values we choose. K_{max}(critical) never exceeds unity so **we can choose K values such that DCM never occurs.** We choose K to give the D value for the CCM to DCM transition.



2. Summary of K_C and R_C for the Big Three

Converter	$K_{crit}(D)$	$\max(K_{crit})$ $0 \le D \le 1$	$R_{crit}(D)$	$\max(R_{crit})$ $0 \le D \le 1$
Buck	(1-D)	1	$2L/(1-D)Ts$	$2L/Ts$
Boost	$D(1-D)^2$	4/27	$2L/D(1-D)^2Ts$	$27*L/2Ts$
Buck-Boost	$(1-D)^2$	1	$2L/(1-D)^2Ts$	$2L/Ts$

The I(critical) value can be made an R(critical) for a fixed output voltage.

$K > K_c$ is CCM $\Rightarrow R < R_c(D)$

$K < K_c$ is DCM $\Rightarrow R > R_c(D)$

For buck D' $\underline{\le}$ 1.0 $\Rightarrow R_{crit} > \frac{2L}{Ts}$ $\therefore$ If $R < R_c$ always CCM

At the CCM to DCM boundary of the DC load current, qualitative and quantitative changes occur in the effective DC transfer. The CCM to DCM border occurs at a value of K called K(critical). K(critical) depends only on the chosen value of D and nothing else. We chose K (circuit values) and f_{sw} to set the D value where the CCM and DCM transition occurs, if desired. The Buck is unique because we can choose K above unity so that DCM never occurs or so that it occurs at some specified D value. Looking ahead to lecture 38 we will prove the table given below.

Summary

Converter	$K_{crit}(D)$	DCM $M(D,K)$	DCM $D_2(D,K)$	CCM $M(D)$
Buck	(1-D)	$\frac{2}{1+\sqrt{1+K/D^2}}$	$\frac{K}{D}M(D,K)$	D
Boost	$D(1-D)^2$	$\frac{1+\sqrt{1+K/D^2}}{2}$	$\frac{K}{D}M(D,K)$	1/(1-D)
Buck-boost	$(1-D)^2$	$\frac{-D}{\sqrt{K}}$	$\sqrt{K}$	-D/(1-D)

The value of D_2 is also listed in terms of K, D and M(D). DCM occurs for $K < K_{crit}$ or CCM occurs for K > K(critical).

DCM operation is controversial.

1. Low value L is required for $\Delta i > I_{DC}$ means lower parts cost . However, larger Δi means larger inductor core losses and perhaps core saturation.
2. Some applications need a natural voltage boost at light load ($R=\infty$) such as self-starting fluorescent lights. However, for a microprocessor power supply any overvoltages at light load could be fatal, if too great.
3. The output voltage is load sensitive unless we employ voltage feedback to overcome this. If PWM dc-dc converters must operate at low power levels DCM behavior must be designed in from the onset.

We then conclude:

1. The discontinuous conduction mode occurs in converters containing current- or voltage-unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse polarity.
2. Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and dc components cause the switch on-state current or off-state voltage to reverse polarity.
3. The dc conversion ratio M of converters operating in the discontinuous conduction mode can be found by application of the principles of inductor volt-second and capacitor charge balance.