LECTURE 16
Bipolar Core Excited Full Bridge and Push-Pull Converters Utilizing 2T_{sw} Timing

I. Full Bridge and Push-Pull Converters
   A. General Issues

   B. Alternating \( \pm V_g \) but balanced Primary Drives:
      \( +V_g \) and zero for first \( T_{sw} \) followed by \( -V_g \) and
      zero for second \( T_{sw} \)

   C. Bridge Rectified Buck with 4 Switch Input
      1. 2T_{sw} drive timing
         a. Primary Conditions D and D’ during
            first \( T_{sw} \)
         b. Secondary Conditions D and D’
            during second \( T_{sw} \)
      2. Input/Output Currents
      3. \( i \) and \( v \) Waveforms over 2T_{sw}
      4. Other 2T_{sw} Switching Schemes

LECTURE 16
Bipolar Core Excited Full Bridge and Push-Pull Converters
Utilizing 2T_{s} Timing
A. General Issues
   1. Power Levels

   The power needs of various electronic power supplies varies as
   shown below.
As the power level changes we also will need to determine which of the big eight PWM converter topologies is best suited to the required power level. Choice of PWM topology will in turn determine the switch stress experienced by the power switches. Moreover, the timing sequence for driving the various topologies will also vary. In particular, we will cover both switches drives at $f_{sw}$ and switches synchronized at $\frac{1}{2} \times f_{sw}$ in our discussions below. On the next page we briefly summarized what we learned in lecture 11 as regards switch topology and power as well as voltage and current levels in the associated switches.
In lectures 16 and 17 we will cover the last of the big eight topologies. We need to employ these circuits to achieve kW power operation. With topology comes different switch stress. That is as the input voltage changes we use different topologies as shown below. The flyback has low parts count but high peak currents than those in a forward converter. The half bridge reduces switch voltage stress because only ½ the $V_{in}$ appears across the primary winding. The full bridge requires four switches, two of which require floating gate drive. The push-pull, as we will see below, also works but has a danger of CORE SATURATION. This could cause us to fry the switch if not careful to balance the core so that no imbalances or DC levels occur.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Power Range (W)</th>
<th>$V_{in\text{(dc)}}$ Range</th>
<th>In/Out Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>0–1000</td>
<td>5–1000</td>
<td>No</td>
</tr>
<tr>
<td>Boost</td>
<td>0–150</td>
<td>5–600</td>
<td>No</td>
</tr>
<tr>
<td>Buck-boost</td>
<td>0–150</td>
<td>5–600</td>
<td>No</td>
</tr>
<tr>
<td>Half-forward</td>
<td>0–150</td>
<td>5–500</td>
<td>Yes</td>
</tr>
<tr>
<td>Flyback</td>
<td>0–150</td>
<td>5–500</td>
<td>Yes</td>
</tr>
<tr>
<td>Push-pull</td>
<td>100–1000</td>
<td>50–1000</td>
<td>Yes</td>
</tr>
<tr>
<td>Half-bridge</td>
<td>100–500</td>
<td>50–1000</td>
<td>Yes</td>
</tr>
<tr>
<td>Full-bridge</td>
<td>400–2000+</td>
<td>50–1000</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Where various transformer-isolated topologies are commonly used.
2. Timing Sequence
To date we have employed switches driven at $f_{sw}$. Today we will change this timing on individual switches to $f_{sw}/2$ so that we can use more switches with less stress per switch as we describe below in more detail

B. Alternating $+V_g$ but balanced Primary Drives:
$+V_g$ and zero for first $T_{sw}$ followed by $-V_g$ and zero for second $T_{sw}$

Bridge type isolated Buck converters are employed with two separate but balanced $T_{sw}$ time periods. This is timing sequence is used for high power converters $P > 1kW$ since we employ twice as many switches to reduce switch stress. Below we will first introduce the concepts via a half bridge and then employ a full bridge with a full analysis.

![Diagram of half-bridge Buck converter](image)

Notice that the two switches alternate in time applying $V_{in}$ alternatively to the transformer primary. Switch voltage stress is
Given by the full input voltage. A similar situation occurs for the full bridge shown below which also alternatively places $V_{in}$ across the primary winding, but this time using four switches.

![Diagram of full bridge converter topology]

We synchronize switches 1 and 4 together in time and then switches 2 and 3. Note that we place the full $V_{in}$ across two switches in series when the timing puts $Sw_{2-3}$ in the same sequence and $Sw_{1-4}$ in the alternative sequence. Hence, we reduce switch voltage stress when we employ the required high input voltage to reach high power levels. Again we have a trade-off as we employ more switches but their individual cost may well be much lower—hopefully a factor of ten.

On the next page we will summarize the switch sequence as well as the voltage ramp on the duty cycle circuit for the full bridge converter topology.
Now we are ready to go step by step through the timing sequence when the primary is driven by + and − \( V_{\text{in}} \) and the secondary is center tapped.

1. **Primary** During balanced drive of duration \( 2T_s \)

   Match components very well to get \( V_{\text{dc}}(\text{offset}) \) on the core zero if the two switch periods are exactly balanced. Use a bridge circuit to drive the input to the transformer alternatively positive and negative. Output of the transformer is center tapped as shown below.
a. First $T_s$ switch interval: $+V_g$ and zero applied sequentially

There are therefore two $T_{sw}$ intervals one with $+V_g$ and one with $-V_g$ across the primary. Below is that during the first $T_s$ in the primary with $+V_g$. $V_T$ switches between 0 and $V_g$ like non-isolated buck as follows during $T_{sw}$. During D $V_g$ is applied and during D’ zero is applied.

**Primary (during first $T_s$)**

<table>
<thead>
<tr>
<th>During D</th>
<th>During D’</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1&amp;Q_4$ on</td>
<td>To achieve</td>
</tr>
<tr>
<td>$V_T = V_g$</td>
<td>$V_T = 0$</td>
</tr>
</tbody>
</table>

\[ V_T = V_g \]
\[ V_T = 0 \]

either of two ways:

1. All $Q_1$-$Q_4$ off, $V_T = 0$
2. $Q_1$, $Q_3$ on, $V_T = 0$

$V_T=0$ via equal V both sides
This means $i_{Lm}$ is flat during D’

b) Second $T_{sw}$ interval: $-V_g$ and zero applied

The primary circuit looked at during the second $T_s$ timing interval is different $T_{sw} \rightarrow 2T_{sw}$ because $-V_g$ is applied during D and zero during D’.
Primary (During $T_s \rightarrow 2T_s$)

**During D**

- **Second Period**
  - $Q_1$ and $Q_3$ on
  - $V_T = -V_g$

**Conditions:**

$$\text{im} \Rightarrow -\frac{V_g}{L}$$

$$\Downarrow$$

$V_T$ switches between $-V_g$ and 0 in primary.

By symmetry we reset the core of the transformer $L_m$ over $2T_s$. Up during D of the first $T_s$ and down during D of second $T_s$.

$$\langle v_{L_m} \rangle_{2T_s} = 0$$

Because of the switching configuration the transformer waveforms are at a frequency $f_s/2$, not at $f_{sw}$.

2. Secondary Voltage $V_s$ Timing:

a) During first $T_s$ interval

- **During D**
  - $V$ on secondaries
  - $nV_g = V_s$
  - * on coils tell
  - diode $D_5$ on and
  - diode $D_6$ off

- **During D’**
  - $V$ on secondaries
  - is zero as $V_T = 0$
  - * on coils tell
  - both $D_5$ and $D_6$ will be on
  - $D_5$ stays on due to $i_L$
  - $D_6$ goes on due to secondary polarity and the dot convention

b) During second $T_s$ interval

Find on your own for D $Q_2$, $Q_3$ and $D_6$ are on while for D’ diodes $D_5$
and D6 are on.

2. Input and output currents

\[ i_{\text{out}} = i_D^5 + i_D^6. \]

How it splits is uncertain, but if at anytime it splits equally then:

\[ i_D^5 = i_D^6 = \frac{i_{\text{out}}}{2} \]

During first \( T_s \) interval \( i_{\text{in}} \) (transformer) = ? When \( i_D^5 = i_D^6 \)

At the output
\[ i_D^5 + i_D^6 \]
while in the primary
\[ i_D^5 \text{ causes } n_i D^5 \]
\[ i_D^6 \text{ causes } n_i D^6 \]

Review the dot convention on a two turn transformer that says:

if \( n_1 i_1 \) is positive \( \Rightarrow +n_1 \) then

is negative \( \Rightarrow -n_2 i_2 \)

\[ n_1 i_1 + n_2 i_2 = 0 \]

coming into the dot in secondary and into dot of primary

At the primary on top of the page we have three currents.
\( i_D^5 \) and \( i_D^6 \) flow in opposite directions with respect to the coil dots:
\( i_{\text{in}} \) and \( i_D^6 \) are assumed flowing into the dot

\[ i_{\text{in}} - n_i D^5 + n_i D^6 = 0 \Rightarrow i_{\text{in}} = 0 \]
flows cancel assuming out of dot if equal \( i_{D5} = i_{D6} \)

For \( i_{in} \) alternating then in general \( i_{D5} \) and \( i_{D6} \) alternate the flows as shown below but always the load receives current either for \( i_{D5} \) or \( i_{D6} \):

\[
\begin{align*}
\downarrow \\
i_1 &= i_{in} + i_M.
\end{align*}
\]

During the first \( T_s \) we find during interval D the two equations below
\[
\begin{align*}
i_m &= i_1 - ni_{D5} + ni_{D6} \} \quad \text{Transformer input} \\
i_{(out)} &= i_{D5} + i_{D6} \} \quad \text{Transformer output}
\end{align*}
\]

During the second \( T_s \) period \( T_s \to 2T_s \) during the same interval D we get the same result for \( i_m \) and \( i_{out} \). Note in the first \( T_s \) with \( +V_g \) applied \( i_{D5} \neq 0 \) but \( i_{D6} = 0 \). Where as in the second \( T_s \) with \( -V_g \) applied \( i_{D5} = 0 \) but \( i_{D6} \neq 0 \).

\[\Rightarrow \text{Switching ripple at } f_s\]
\[\Rightarrow \text{Transformer ripple occurs at } f_s/2!\]
3. Selected i and v waveforms vs $2T_s$ in the Bridge Converter

\[ V_g/L_m - V_g/L_m \]

\[ V_g - V_g \]

\[ i(t) \]

\[ \Delta i \]

\[ v_s(t) \]

\[ nV_g - nV_g \]

\[ i_D(t) \]

\[ i - 0.5i - 0.5i \]

\[ 0 - DT_s - T_s - T_s + DT_s - 2T_s \]

\[ \text{conducting devices: } Q_1, Q_4, D_5, D_6, Q_2, Q_3, D_5, D_6 \]

\[ < V_{Lm} > 2T_s = 0 \]

unless small offsets occur

\[ V_o = < V_s > 2T_s = nDV_g \]

Clearly $Q_1$ and $Q_2$ cannot both be on at the same time nor $Q_3$ and $Q_4$ or $V_g$ is shorted all other commutations are possible. $D_1$ and $D_2$ clamp the primary to a maximum of $V_g$. Note bipolar use of the primary $l_{LM}$ winding. The center tapped secondary winding is unipolar since in each half cycle alternate coils conduct.
4. Other switching schemes over a $2T_s$ period are also possible that include.

1. Alternative polarities applied to $V$(primary) during 1st and 2nd $T_s$ periods for duration $DT_s$.

2. A dead active switching period during both 1st and 2nd $T_s$ periods, where all switches are off.

\[ T_1, T_2 \]
\[ V_o \]
\[ V_d \]
\[ + \]
\[ - \]
\[ + \]
\[ - \]
\[ + \]
\[ - \]
\[ + \]
\[ - \]

Explore this possibility for an extra credit HW assignment.

5. Switch Stress Review

<table>
<thead>
<tr>
<th>Estimating the Significant Minimum Parameters of the Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductors</td>
</tr>
<tr>
<td>Topology</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Half-bridge</td>
</tr>
<tr>
<td>Full-bridge</td>
</tr>
</tbody>
</table>

Above the half and full bridge switch stress are estimated.
C. Push-Pull Transformer Isolated Buck

1. Circuit Topology and Timing
We first show a brief sketch of circuit waveforms in the push-pull circuit. The secondary is the same as the full bridge converter. Here however, the primary winding is also center-tapped. Notice that the switch voltage stress is nearly $2V_{in}$ and the switches alternatively conduct the current to the two portions of the center tapped primary winding. When one switch is on the other is off. On the next page we rearrange the schematic and do a full blown analysis to capture circuit waveforms at $f_{sw}/2$, with full cycle duration of $2T_{sw}$. 

![Circuit Diagram]

The push-pull regulator topology.
There are two periods of duration $T_s$ per full cycle. In the first $Q_1$ is on for D while in the second $Q_2$ is on for D.

1st $T_s$
- $Q_1$ on for D putting $+V_g$
- on upper half of primary
- but with + on un-dot side
- Causes $+V_s$ on
- upper right secondary

2nd $T_s$
- $Q_2$ on for D putting $+V_g$
- on lower half of primary
- with + on dotted side
- Causes $+V_s$ on
- lower secondary

As regards the transformer $L_m$ we find:

1st $T_s$: Builds up $i_m$

2nd $T_s$: Reduces $i_m$

$V_o = nDV_g$ for DC conditions.
2. i and v waveforms vs $2T_s$

$\langle V_{Lm} \rangle_{2T_s} = 0$

$V_0 = \langle V_s \rangle_{2T_s} = nD V_g$

$Q_1$ is on first $T_s$ for $DT_s$ and $Q_2$ is on second $T_s$ for $DT_s$ but are $Q_1$ and $Q_2$ the same? If not, What might occur? How we might avoid this core saturation is given below in section 3.
First we review the switch stress of the push-pull compared to the half and full bridge covered earlier.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Bipolar Power Switch</th>
<th>MOSFET Power Switch</th>
<th>Rectifier(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{CEO}$</td>
<td>$I_C$</td>
<td></td>
</tr>
<tr>
<td>Push-pull</td>
<td>$2V_{in}$</td>
<td>$\frac{1.2P_{out}}{V_{in(min)}}$</td>
<td>$2V_{out}$ $I_{out}$</td>
</tr>
<tr>
<td>Half-bridge</td>
<td>$V_{in}$</td>
<td>$\frac{2P_{out}}{V_{in(min)}}$</td>
<td>$2V_{out}$ $I_{out}$</td>
</tr>
<tr>
<td>Full-bridge</td>
<td>$V_{in}$</td>
<td>$\frac{1.2P_{out}}{V_{in(min)}}$</td>
<td>$2V_{out}$ $I_{out}$</td>
</tr>
</tbody>
</table>

Note that the push-pull is equivalent to the full bridge in switch stress and better than the half bridge. However, the push-pull is a dangerous circuit as it has a tendency towards core saturation which will cause the transformer input to look like a short and will likely kill the switches. This arises when the flux within the core is inadvertently non-symmetric so that a small DC offset occurs. Unfortunately, this small offset will cause a walk towards saturation over many switch cycles. Usually, current mode feedback must be employed rather than voltage feedback to control this difficulty of push-pull. Also possible, is active core rebalancing as illustrated on the next page.
3. Push-Pull Transformer Balance Problem

To monitor SATURATION of Transformer Core we will employ current sensors in $Q_1$ and $Q_2$ collector's to look for high current spikes.

We compare to $I_{\text{control}}(\text{ref})$ and we shut off $Q_1$ and/or $Q_2$ if $I > I_{\text{control}}$.

Due $V_{\text{on}}(Q_1) \neq V_{\text{on}}(Q_2)$ and $\Delta t (Q_1) \neq \Delta t(Q_2)$ we might have a slight offset each clock cycle and $i_{Lm}$ is not zero.
Even a small imbalance adds up after 100 switch periods and the transformer will ultimately saturate. Then for example the current on $i(Q_1)$ will shoot up when $L_m \rightarrow 0$

Use $I_c$ (control) as a maximum to sense if $i_{Q1}$ gets excessive and shut it down if it does. In practice we never build push pull converter with duty cycle control and voltage. Rather we use current programmed control of Chapter 11. Below we compare switch stress in the topologies of lectures 15 and 16.
Estimating the Significant Minimum Parameters of the Power

<table>
<thead>
<tr>
<th>Semiconductors</th>
<th>Bipolar Power Switch</th>
<th>MOSFET Power Switch</th>
<th>Rectifier(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
<td>$V_{CEO}$</td>
<td>$I_C$</td>
<td>$V_{DSS}$</td>
</tr>
<tr>
<td>Flyback</td>
<td>$1.7V_{in(max)}$</td>
<td>$\frac{2P_{out}}{V_{in(min)}}$</td>
<td>$1.5V_{in(max)}$</td>
</tr>
<tr>
<td>One Transistor Forward</td>
<td>$2V_{in}$</td>
<td>$\frac{1.5P_{out}}{V_{in(min)}}$</td>
<td>$2V_{in}$</td>
</tr>
<tr>
<td>Push-pull</td>
<td>$2V_{in}$</td>
<td>$\frac{1.2P_{out}}{V_{in(min)}}$</td>
<td>$2V_{in}$</td>
</tr>
<tr>
<td>Half-bridge</td>
<td>$V_{in}$</td>
<td>$\frac{2P_{out}}{V_{in(min)}}$</td>
<td>$V_{in}$</td>
</tr>
<tr>
<td>Full-bridge</td>
<td>$V_{in}$</td>
<td>$\frac{1.2P_{out}}{V_{in(min)}}$</td>
<td>$V_{in}$</td>
</tr>
</tbody>
</table>