LECTURE 4

Introduction to Power Electronics Circuit Topologies: The Big Three

I. POWER ELECTRONICS CIRCUIT TOPOLOGIES
A. OVERVIEW
B. BUCK TOPOLOGY
C. BOOST CIRCUIT
D. BUCK-BOOST TOPOLOGY
E. COMPARISION OF THE BIG THREE

II. TOPOLOGY OF L-C OUTPUT FILTERS
A. C ALWAYS Located ACROSS $V_{out}$
B. L LOCATED BETWEEN CRUDE UNFILTERED $V_{dc}$ AND STABILIZED $V_{out}$
   1. BUCK
   2. BOOST
   3. BUCK-BOOST
   4. LOW RIPPLE APPROXIMATION FOR OUTPUT SIGNALS AT $f_{sw}$
      a) INDUCTOR RIPPLE:
         \[ \Delta i = \frac{V}{L} dt\text{(switch)} \]
      b) CAPACITOR RIPPLE:
         \[ \Delta V = \frac{I}{C} dt\text{(switch)} \]
         \[ dt\text{(switch)} = (Duty \ cycle) \times T_s \text{(period of } f_{sw}) \]
Introduction to Power Electronics Circuit Topologies: The Big Three

A. OVERVIEW
The Inductor in any PWM converter plays the role of a mechanical flywheel in that it stores energy between pulses. The solid state switches pulse energy at the switching frequency into the PWM circuit from the input but the inductor stores energy so that the energy drawn to the load does not appear pulsed at all. We will see below that both the precise location of the inductor in the circuit topology as well as the physical location of the switch on the specific terminal of the inductor are crucial to realize the three major PWM circuit topologies. The inductor – switch combination will have three unique topological locations. In section B, for simplicity, we will use the three major topologies to convert a DC input to various DC outputs that are both below and above the original V(in) in voltage. We will express the steady state transfer function of all converters as a function of the duty cycle: F(D)

B. BUCK TOPOLOGY

(a) BUCK TOPOLOGY: Inductor attached to c in series. note how l avoids kvl violations for brief periods by acting as a buffer between vin and vot as well as storing energy.

![Diagram of Buck Topology]
• $V_{\text{out}}/V_{\text{in}} = D(\text{DUTY CYCLE}): v(\text{out}))$ has a linear dependence on $d$; $v_{\text{out}}$ never exceeds $v_{\text{in}}$

• Below we qualitatively outline the analysis of the BUCK circuit both for the switch on and off

In lectures 5-7 we will go through this circuit in detail for now be sure to see the very different circuit for the two switch conditions on the bipolar transistor. The diode because of its bipolar nature is a switch that does not need to be actively driven by a gate drive.
B. BOOST TOPOLOGY:
Inductor is attached to crude dc (rectified mains): again note that L is preventing kvl violations during switching as well as storing energy.

\[ V_{out}(\text{minimum}) = V_{dc} \]
and can exceed \( V_{dc} \)

\( V_{out} \) IS UNIPOLAR but can achieve \( v_o > v_{in} \)

\( V_o/V_{in} = 1 / (1-D) \). non-linear dependence on \( d \)
will be shown in later lectures

Note that the input and the output are NOT electrically isolated from each other as we have a common terminal to both the input and the output. How to easily fix this?? Finally, we consider one special case for the duty cycle- \( D=1/2 \)

Consider the switch duty cycle of \( 1/2 \) and consider the power in the inductor for each switch position.

\[ p_{in}(av) = v_{dc}i/2 \text{ while } p_{out}(av) = (v_{out} - v_{dc})i/2 = p(\text{inductor}) \]
if no losses occur in switching, wires or in reactive elements: \( p_{in}=p_{out} \) which implies \( V_o=2V_{dc} \).

On the next page we give a qualitative summary of the boost topology for the conditions of the bipolar transistor switch on and off. Note the very different current paths for the two circuit conditions. Of special note is the inductive kick from the series inductor which makes the switch voltage exceed \( V(in) \) when the transistor is switched off. Why does this occur??
For now realize that the boost circuit while delivering an output voltage above $V_{\text{in}}$ does have to ask the solid state switch to handle a peak current 6 times the nominal average current when the switch is on. When the switch is off the solid state switch must withstand across itself a voltage up to the full output value.
C. BUCK-BOOST TOPOLOGY:

Inductor is connected in parallel with C which acts as a polarity reverser. Given \( +v_{dc} \) as input in we generate \(-v_{dc}\) out for a switch duty cycle of \( \frac{1}{2} \). Many analog circuits require both \(+\) and \(-v_{dc}\) supplies and this is an easy way to do it.

\[ V_{DC} \quad \text{V}_{\text{OUT}} \]

the inductor I again avoids kvl violations by acting as a current source temporarily.

- \( V_{\text{out}} \) (MINIMUM) IS NOW ZERO
- \( V_{\text{out}} \) IS OPPOSITE POLARITY TO \( v_{dc} \) due to current direction in the inductor that charges the c.

\[ \int \frac{V_{dc}}{L} \, dt = \Delta i_L \Rightarrow i_L \text{ DOES NOT CHANGE} \]

instantaneously so the capacitor charges negatively.

- FOR BUCK-BOOST EITHER \( |V_{\text{out}}| > V_{dc} \) OR \( |V_{\text{out}}| < V_{dc} \) IS POSSIBLE
- \( V_{\text{out}} / V_{\text{in}} = -D / (1-D) \). non-linear dependence on d will be shown in lectures 5-7

On the following page we show schematically the waveforms for the buck/boost circuit for both the switch on and the switch off. Again the ability to generate voltages above the input voltage comes at the price of expensive solid state switches. With the switch on we need to pass nearly 6 times the average current. With the switch off we need to stand off across the switch \( V(\text{in}) + V(\text{out}) \).
In preparation for your midterm exam, look at the attached schematic on pg. 8 of a flyback converter slowly - don't panic. try to find only the essential power electronics portions.

1) Identify the crude dc generation in the upper left driven by 120 ac mains. this CRUDE DC is DRIVEN BY THE SWITCH #1 INTO THE TRANSFORMER PRIMARY.

2) On the right side of the schematic notice the three secondaries of the transformers with the three dc outputs: 5, 12, and 30 v.

3) Find the cmos transistor Q1 (middle) which is the switching transistor. From the gate of this cmos switch the gate control circuitry may also be found.

We will spend the rest of the semester detailing how such circuits work.
D. Full Monty Comparison of the Big Three Topologies

Below we place three tables that compare the BUCK, BOOST, and BUCK/BOOST topologies as regards:

- Expected Loss in percent from the three topologies
  1. Rectifiers of the output
  2. The solid state switch
  3. The magnetic core material in inductors as well as core material in transformers
  4. Miscellaneous loss such as wire losses, parasitic losses and radiative loss

- Estimate the requirements of the switches both when on and when off. Details later!
Again the purpose of the above tables is to illustrate that the choice of topology has a major impact on the tradeoffs involved in design. We want to do this as early as possible so one is aware of this from the start. We will in fact derive in later lectures many of the parameters simply given above. Still it is worthwhile to compare even now.

**Next we outline a building block design approach.**
From the above approach we need to pick a starting point. We will focus next of the output filter design in the remainder of this lecture and in lectures 5 and 6.

E. BASIC TOPOLOGIES OF PASSIVE L-C FILTERS

We will use L-C filters both to remove $v_{ac}$ signals lost to conversion and to avoid kvl and kil law violations from the switching.

1. DC OUTPUT REACTIVE FILTER (L-C). This places a series $L$ between two voltages sources $v_{in}$ and $v_{out}$. It also removes or reduces the switch signal at $f_s$ and passes only dc if designed properly. Let's look at the two
pieces of an L-C filter separately for clarity of each role. first the output capacitor.

a. **FIXED CAPACITOR LOCATION: C ALWAYS PARALLELS R_L**

![Circuit Diagram]

- C is in parallel with $v_{\text{out}}$
- $\Delta v_{\text{out}}/v_{\text{out}}$ is the quantitative regulation desired, $i_c = c*dv_c/dt$
- $\Delta V_{\text{cap}} = \int \frac{i_{\text{out}}}{C} \, dt \Rightarrow V_c$ DOESN'T CHANGE INSTANEOUSLY. It takes time to do so. The time scale of interest is some function of $t_{\text{sw}}$. $\Delta v \sim i/c \, dt$ which implies for fixed i, $\Delta v$ is smaller for large CAPACITOR values. for crude estimates of the desired C values, use the linear approximation. If given or specified the $\Delta v$ value allowed, $i_{\text{out}}$ required, and dt from $f_s$, we can determine proper “C” in a quick calculation.

b. **VALUE OF L DESIRED**

- **INDUCTOR IS OFTEN IN SERIES WITH $V_{\text{dc}}$ AND $V_{\text{out}}$ FOR A BUCK CIRCUIT**

$$V_{\text{dc}} \quad V_{\text{out}}$$

$V_L = Ld(i_L)/dt \quad \int \frac{V_{\text{dc}} - V_{\text{out}}}{L} \, dt = \Delta i_L$
It is a fraction of $t_s - \Delta t_s$ or $d't_s$
given $v_{dc} - v_{out}$ (fixed) and $dt$ (switch) for a specified $\Delta i_l$
variation we fix $l$. Over a cycle of $f_{sw}$ the $\Delta i_l/i_{out}$ can be
specified. We can then fix the required “$l$”. Higher $f_s$ and
smaller $dt$ allows for smaller “$L$”. For compact and light
power supplies small $L$ is a desired goal.

C. CONSIDER $\delta$ FUNCTION CURRENT
CHARGING OF A CAPACITOR, $C$, TO $V_o$ AT $f_{sw}$
The $v_{out}$ will display RC decay in between $\delta$
function charging due to load dc current

If this $\delta$ function charging occurs via a wire with stray
inductances which are typically 5nf/cm at high
frequencies, then the switching waveform would then
appear as a decaying sinusoid with both overshoot and
undershoot at a frequency $w = \frac{1}{\sqrt{LC}}$ and decay envelope
with

$\tau = RC$
**HW#1: Thinking question #2**

Give some general trends for the small ripple approximation in a simple L-C output filter for increasing switch frequency $f_{sw}$ (i.e. smaller $t_s$). Show that a smaller “C” is allowed for fixed I drawn at the load and chosen $\Delta v$ levels. Do a similar argument for the inductor size required.

Now we can better appreciate the following chart which tries to depict all the aspects of ee that power electronics brings together to work on one topic energy conversion: controls, power, parasitic elements, and electronic devices to name a few.

![Chart depicting the interrelation of controls, power, and electronics](chart.png)
OUR TWO SEMESTER COURSE as regards use of Erickson’s text will be as follows. ALL HW PROBLEMS WILL BE FROM ERICKSON

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10 SPRING DISCONTINUOUS MODE
VOLTAGE FEEDBACK:
SIMPLIFICATIONS AND
STABILITY ISSUES,
\( V_{\text{out}} = f(D, \text{LOAD}) \)

11 SPRING CURRENT FEEDBACK
CONTROL: CONTINUOUS OR
DISCONTINUOUS MODES

12, 13, 14 FALL MAGNETICS DESIGN OF
INDUCTORS & TRANSFORMERS

15 SPRING HARMONICS AND HARMONIC
POLLUTION

16-18 SPRING LOW HARMONICS RECTIFIER

19 SPRING ZERO V, I SWITCHING TO
MINIMIZE SWITCHING LOSS

GRADING:
1. HOMEWORK 60 percent-with 10 points from each
chapter 2, 3, 4, 12, 13, and 14
2. Midterm exam 20 percent
3. TERM PAPER 20 percent with 10 extra points for
special projects