EE550

Homework 1

Due March 2, 2006

1. Construct a table listing the bus cycles a 68020 goes through in carrying out the data transfer operation corresponding to

   MOVE.W (A1)+, (A0)

   given that A0 = $ FFFF 0002, A1 = $1000 0000. The system memory is such that memory addresses $00000000 to $C0000000 are in 8 bit wide memory and the rest of the locations are in a 16-bit wide memory. The contents of memory locations are as follows:

   ($10000000) = $00112233
   ($10000004) = $44556677
   ($FFFF0000) = $ABCDDBCA
   ($FFFF0004) = $EFEFEFEF

   For each bus cycle, indicate the contents of the address bus, SIZ0, SIZ1, DSACK0, DSACK1 lines.

Cycle no.	Address	Data	SIZ1,SIZ0	DSACK1,DSACK0
1				
2				