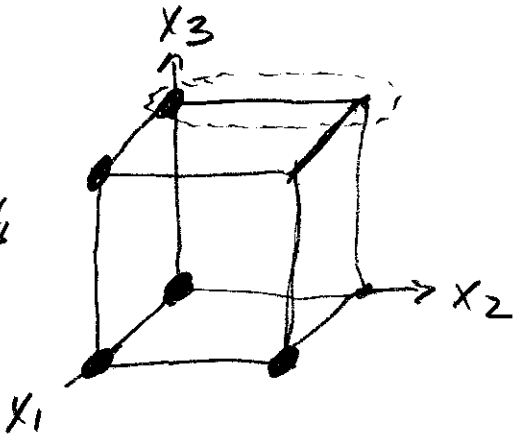
2-16

"Containment"

Cube A_0 contains cube $A_0\bar{A}_1$

2-17

Implicants & Prime Implicants



Implicant: cube containing only ON-SET, DC-SET pts.

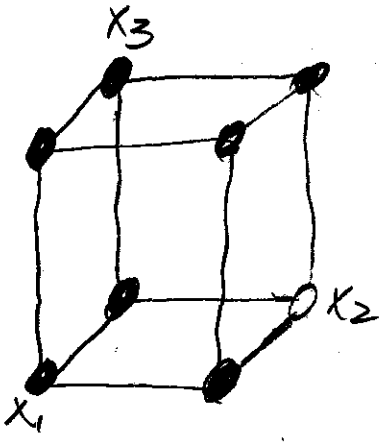
$f_1 = X_2' + X_1X_3'$

PI: a cube (pt, line, sq, ...) not contained by other cube

2-19

EPI

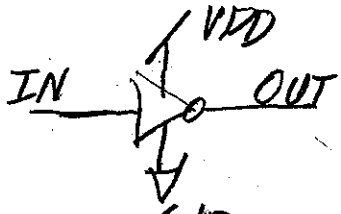
- One or more vertices not contained by another PI
- Non-essential PI?
- EPI(s) must be included in minimized expression (SOP)



Positive True (Active High) vs Negative True (Active Low) Signal Polarity.

Katz

	Sig State	Logic Level	Voltage
Active High	Asserted (active)	1	H
	De-asserted (inactive)	0	L
Active Low	Asserted	1	L ↖
	Deasserted	0	H ↙



← 2 interpretations

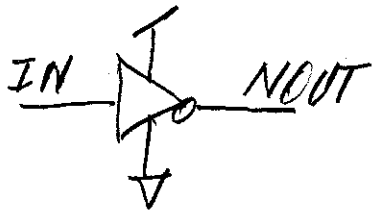
① OUT (AH) = ~IN (AH)

or ② OUT (AL) = IN (AH)

(bubble ≡ AH ⇄ AL)

Wakerly

Active Low	Asserted ↖	0	L
	Deasserted ↙	1	H ~ same as AH



NOUT = ~ IN

(AL) (AH)

This interpretation is compatable with verilog and also allows conversion AH ⇄ AL via bubble.

"Rules" for Dealing w/ Sig Polarity

1) Logic Gate symbols always have same TT (logic symbol fn)

≡

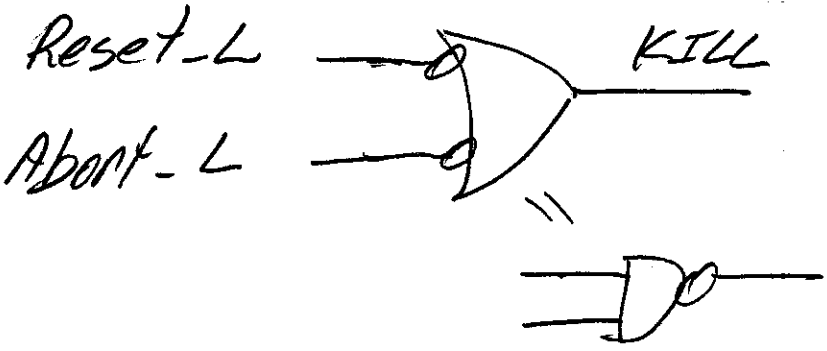
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

2) Indicate signal polarity (AH/AL) by naming convention.

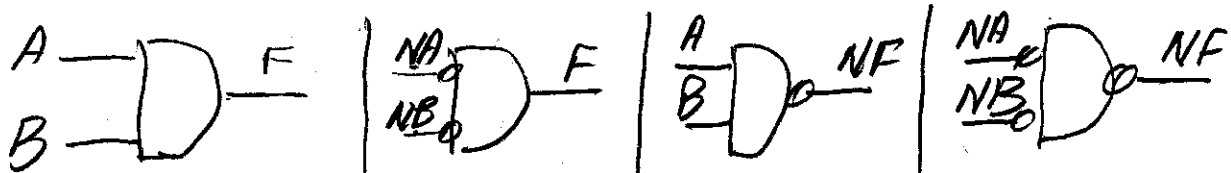
Verilog - compatable N_OUT or OUT_L

3) Everything inside of a logic gate (AND, OR, ...) is Active High

4) Use bubbles to convert inputs to Active High if needed. A bubble on output will convert back to Active Low if needed.



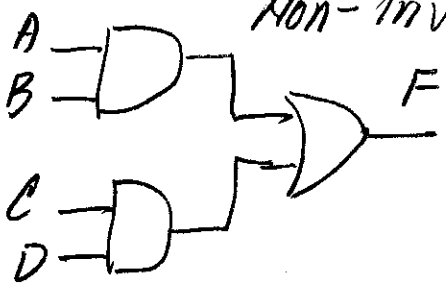
4 Ways to Make an AND



Input Pol	AH	AL	AH	AL
Output Pol	AH	AH	AL	AL

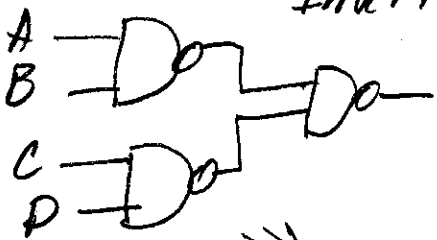
"Bubble Matching"

Non-inverting gates

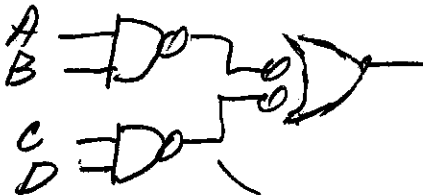


$F = AB + CD$

Inverting gates - CMOS - NANDS



same ckt transformed to match bubbles



Bubbles "cancel"