EE450/EE451-Cadence Tutorial

1. Environment setup

a. Use putty and run Start-X-Windows to log into Linux server, these two programs should in your windows start menu

b. Make sure you are in your home directory

pwd

Check the path, should be:

/top/students/ UNGRAD/ECE/your name/home

c. Create a folder for EE451/450

mkdir EE451

cd EE451

b. Copy and run setup file:

cp /top/students/GRAD/ECE/weiwei/shared/EE451/cadence_setup.sh .

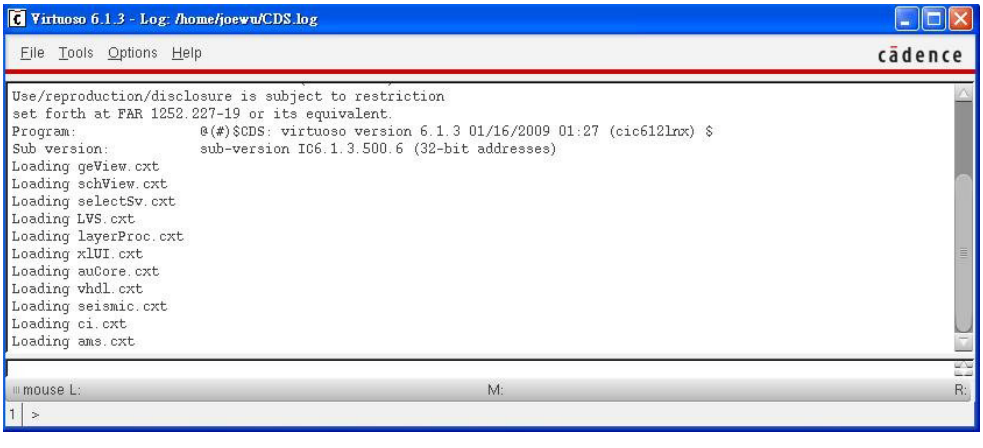
cadence_setup.sh

c. Source Virtuoso

source cust_ic613_mmsim.cshrc

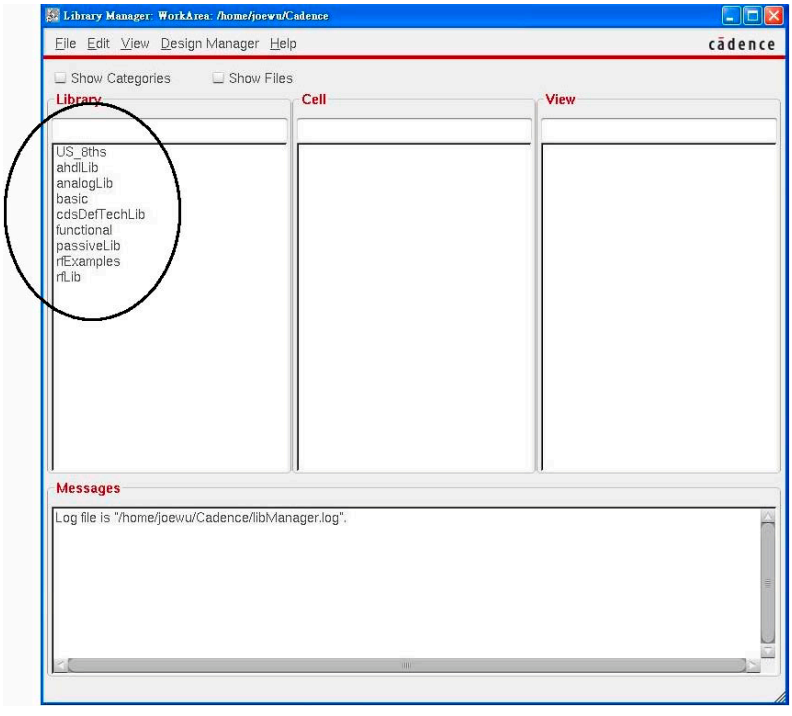
d. Invoke Virtuoso

virtuoso



2. Command Interface Window and Library Manager

a. CIW Some default libraries and the libraries you created will be shown here.
Tools -> Library Manager…

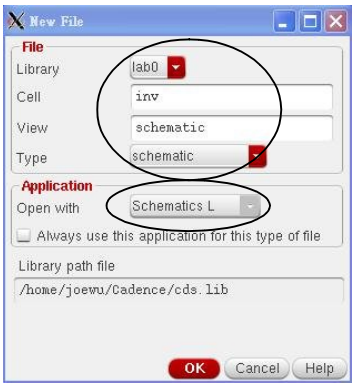


We don't have any gate level schematic in our library, so you need to create the gate from transistor level in your library, save it and use it in the future.

b. Create new library
File -> New -> Library…
Pick a name for the library (name it using your name, for example "Henry", “lab0” in this tutorial).

Check “Compile an ASCII technology file” and browse to tsmc18.tf in the tsmc018_process directory). Close the library manager.

c. Create new schematic
File -> New -> Cell View…
Pick a name for this new cell (“inv” in this tutorial).
Select “schematic” as the Type. Select “Schematics L” in the Application pull-down list.

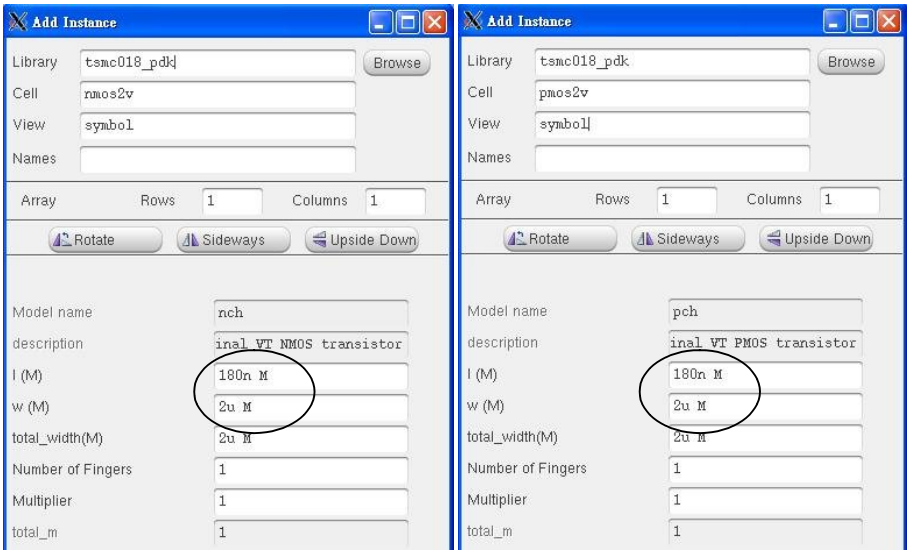


3. Schematic editor

a. Add an instance

Create -> Instance… or click  on the toolbar.

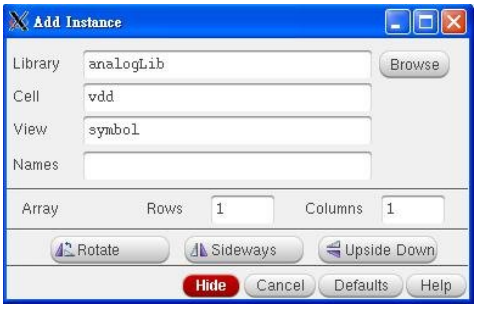
Browse to the cell you want to add to the schematic (select “symbol” as view).
In this tutorial we need a NMOS and a PMOS, they are both in the tsmc018_pdk library. Use “nmos2v” for NMOS and “pmos2v” for PMOS.
The instance property window should pop out. Fill in the necessary information for the instance. Here we need to fill in the “Width” and “Length”.

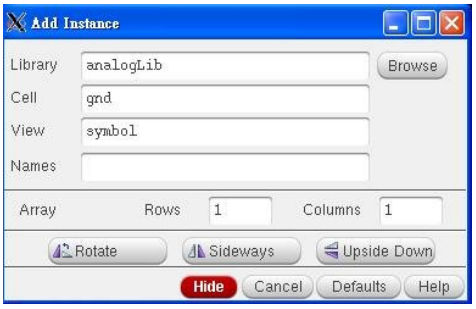


Place the instance by clicking on the schematic drawing window. You can place the same instance as many times as you want by clicking multiple times on the drawing window, press ESC to leave the add-instance mode.

b. Add VDD and Ground

Use “vdd” and “gnd” in analogLib for VDD and Ground, respectively.





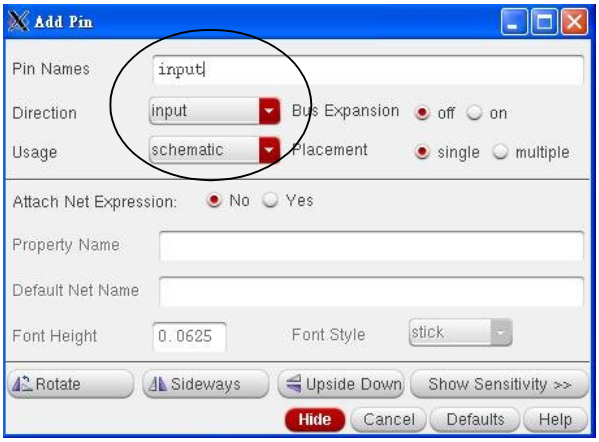
c. Add a pin

Place pins to inputs and outputs nodes.

Create -> Pin… or click  on the toolbar.

Enter the pin name and the direction. In this tutorial we need an input pin and an output pin.

Place and connect them correctly in the schematic.



d. Add a wire

Create -> Wire (narrow) or click  on the toolbar.

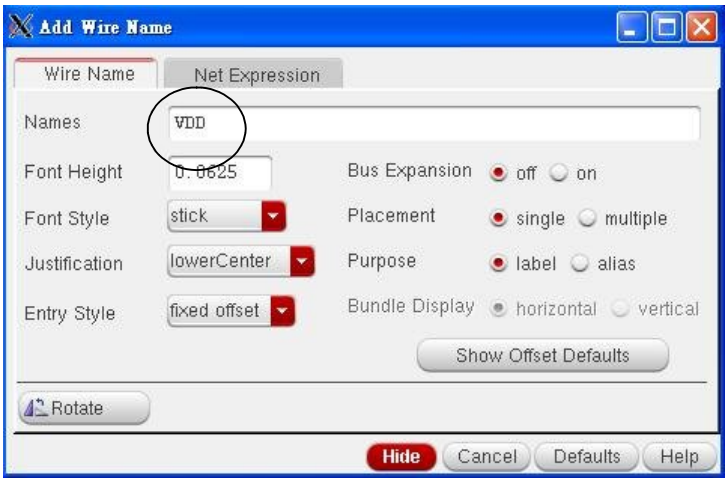
First a single click to start wiring, if this wire ends up at a node of an instance or any part of a wire, a single click to end wiring, otherwise double click to end wiring.

Press ESC to leave wiring mode.

We can rename any nets as we want.

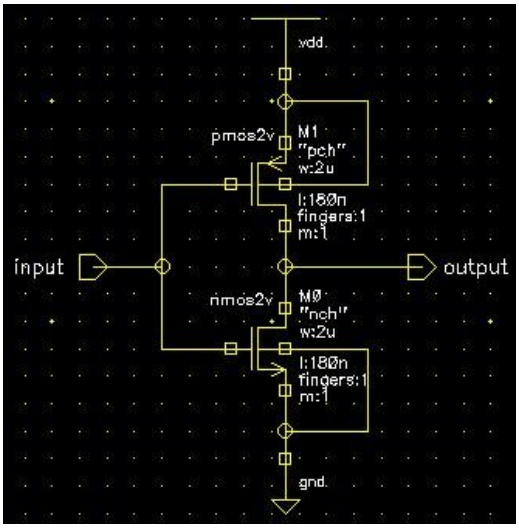
Create -> Wire Name… or click  on the toolbar.

Enter the Wire Name and click on the net you want to rename in the schematic window.



e. Check and Save

The schematic view of the inverter is shown below. Before going any further we need to check the schematic, fix any errors or warning if there are any, and save it.

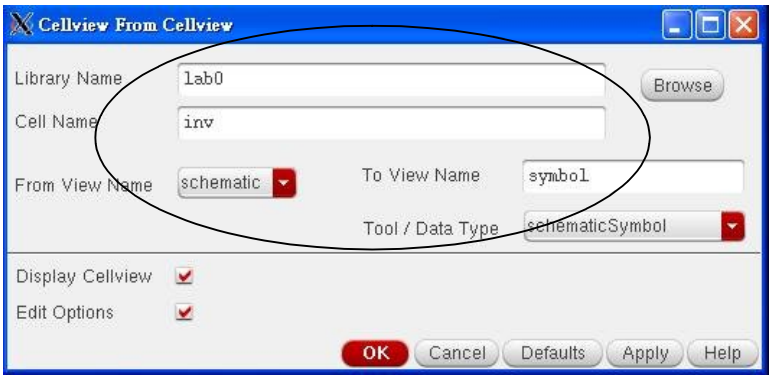


Check -> Current Cellview or click  on the toolbar.

f. Create the symbol view

Create a symbol view for a schematic is good when you do hierarchical design. It makes the schematic clean and easy to understand especially when you have lots of blocks in your design.

Create -> Cellview -> From Cellview…



You can specify the library name, cell name and pin locations of the symbol. The symbol view is shown below.

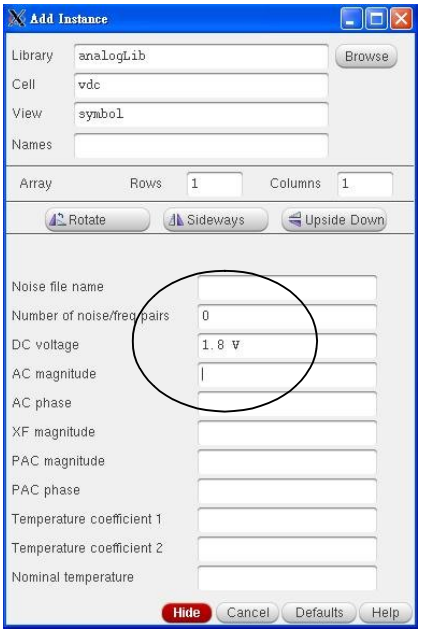
Remember to do “Check and Save” before leaving symbol editor.

Now we have to create a new cellview for top-level design. In this new cellview add the inverter symbol we just did in the schematic.

g. Add power supply

Use a DC voltage source as the power supply.

It is “vdc” in analogLib, place it in the schematic and connect it to “vdd” symbol.

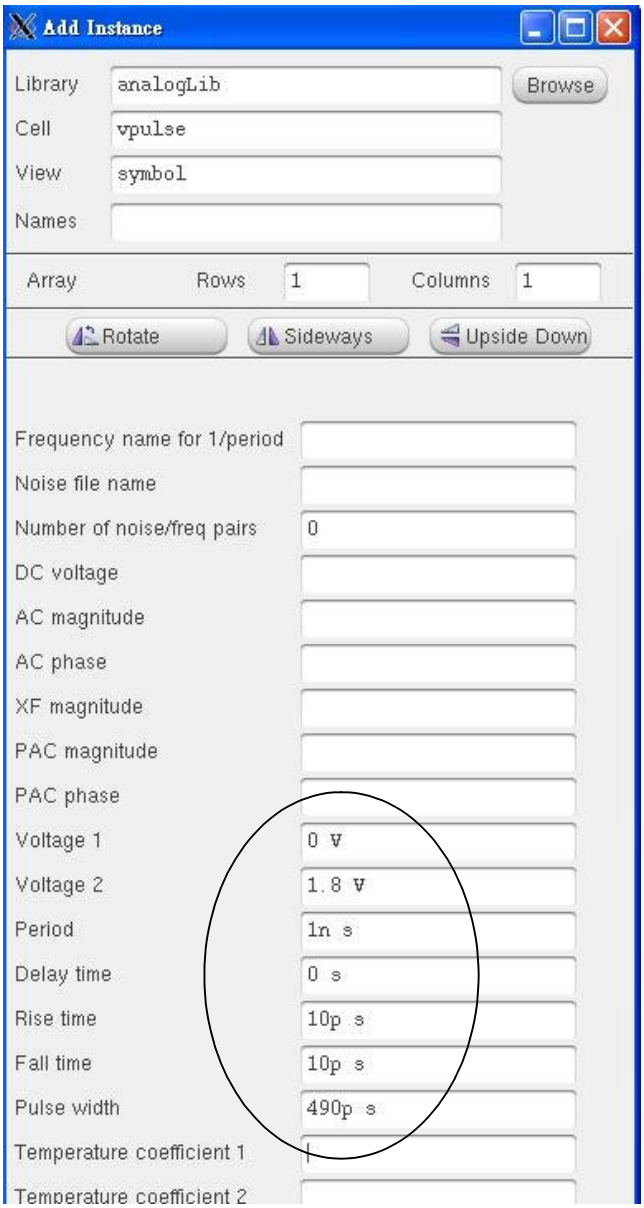


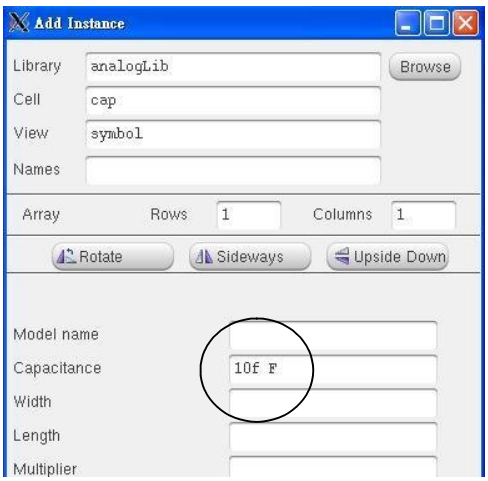
h. Add a stimulus

Here we can use a voltage pulse generator as the input. It is “vpulse” in analogLib. Place it to the schematic and connect it to the input.

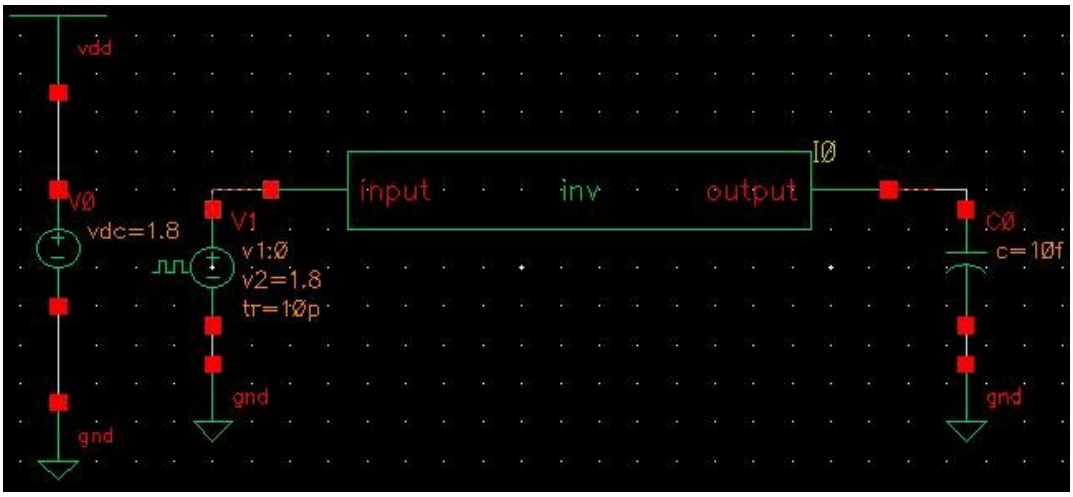
In this tutorial we also need a capacitor at the output. Use “cap” in the analogLib with 10fF as its capacitance.

Place it to the schematic and connect it to the output.





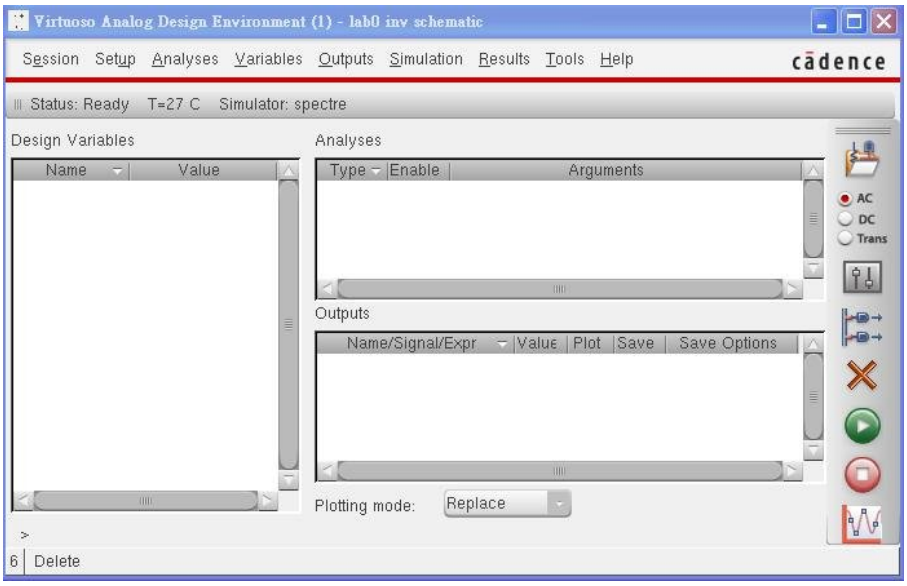
The top-level inverter view is shown below.



4. Spectre - Spice Simulator

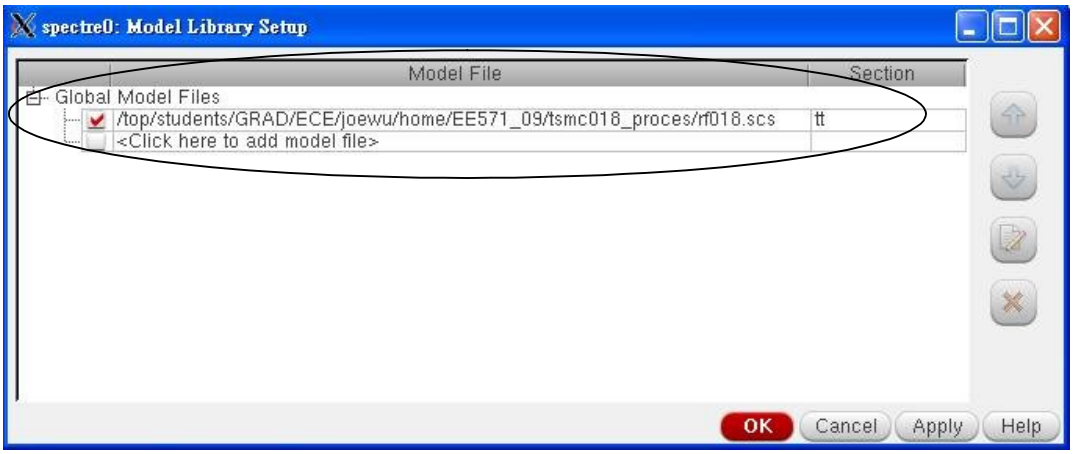
After the schematic is done, we need to test its functionality and performance by running spice simulations. This is done by Spectre.

Launch -> ADE L



a. Setup the library

Setup -> Model Libraries…



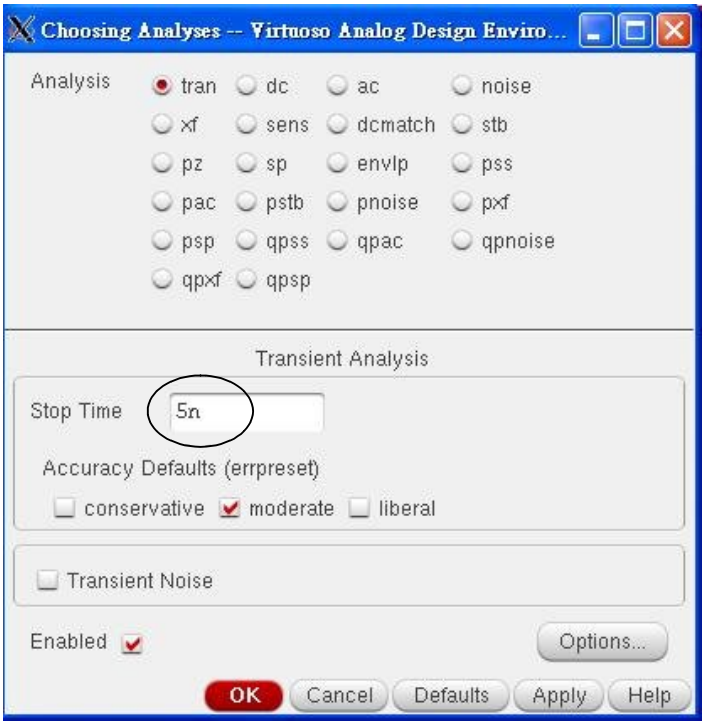
Browse to the library/libraries you want to use for SPICE simulation. In this lab we use “rf018.scs”.

Select “tt” in the Section pull-down list.

b. Add an analysis

Analyses -> Choose… or click 

on the toolbar



There is a list of analyses we can choose from, and associated to each analysis there is a set of options.

Here we only do transient analysis on the inverter. Set the stop time to 5nS.

c. Add a probe

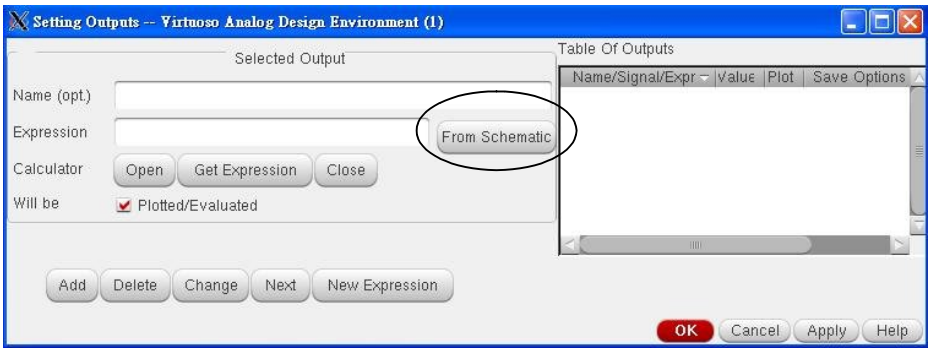
In order to check the waveforms of nets we have to add probes to nets based on our needs. The waveforms will tell us if the functionality is correct and if the performance meets the SPEC.

Outputs -> To Be Plotted -> Select On Schematic

Click on the nets you want to plot. Those nets should be shown in the “Outputs” box in the ADE window.

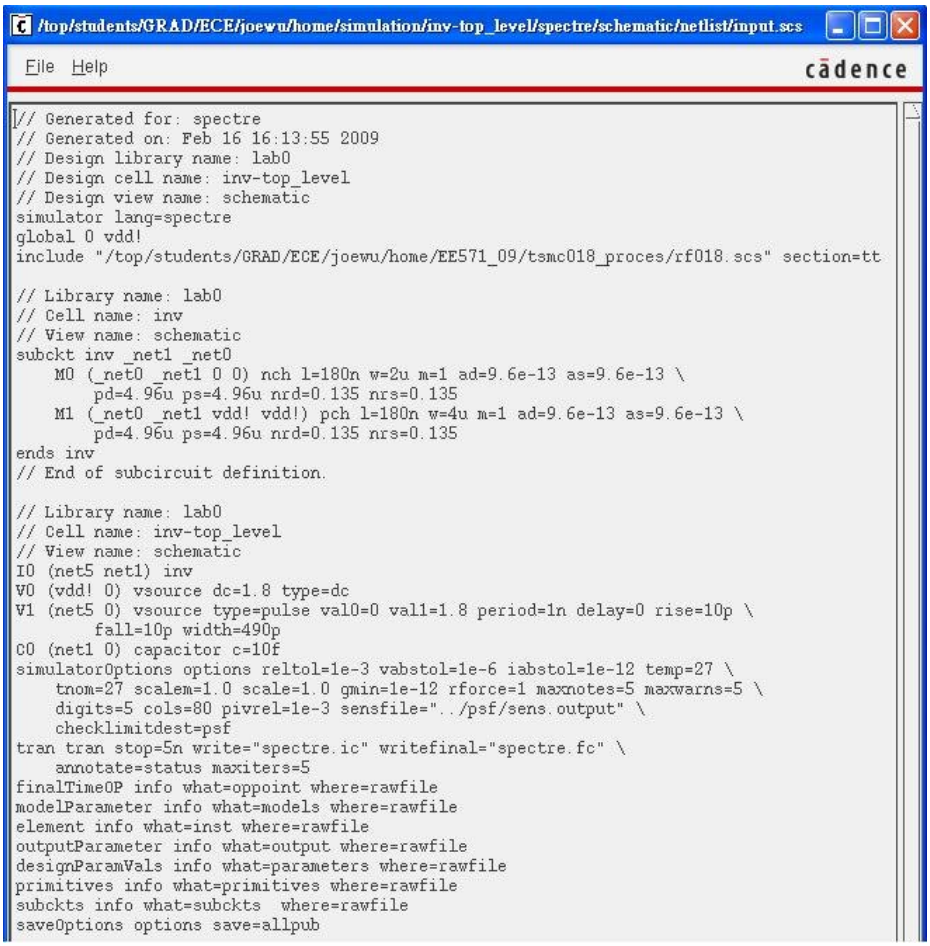
We also can do this by clicking  on the toolbar.

You can enter the net name by hand or select it from schematic view by clicking “From Schematic”.



d. Generate the netlist

Simulation -> Netlist -> Create



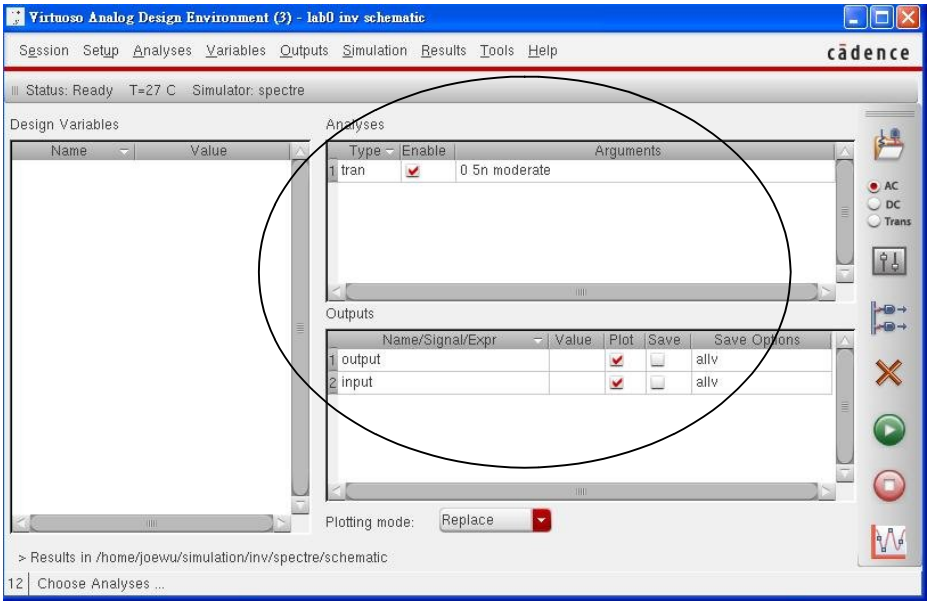

```
// Generated for: spectre
// Generated on: Feb 16 16:13:55 2009
// Design library name: lab0
// Design cell name: inv-top_level
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/top/students/GRAD/ECE/joewu/home/EE571_09/tsmc018_proces/rf018.scs" section=tt

// Library name: lab0
// Cell name: inv
// View name: schematic
subckt inv _net1 _net0
    M0 (_net0 _net1 0 0) nch l=180n w=2u m=1 ad=9.6e-13 as=9.6e-13 \
        pd=4.96u ps=4.96u nrd=0.135 nrs=0.135
    M1 (_net0 _net1 vdd! vdd!) pch l=180n w=4u m=1 ad=9.6e-13 as=9.6e-13 \
        pd=4.96u ps=4.96u nrd=0.135 nrs=0.135
ends inv
// End of subcircuit definition.

// Library name: lab0
// Cell name: inv-top_level
// View name: schematic
I0 (net5 net1) inv
V0 (vdd! 0) vsource dc=1.8 type=dc
V1 (net5 0) vsource type=pulse val0=0 val1=1.8 period=1n delay=0 rise=10p \
        fall=10p width=490p
C0 (net1 0) capacitor c=10f
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=5n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub
```

e. Run simulation

The ADE should be setup as below.



Simulation -> Netlist and Run or click  on the toolbar.