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ModelSim v5.7 Quick Reference Guide

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Background: This guide provides you with step-by-step procedures in using ModelSim to compile, link and simulate your VHDL or Verilog source code design. *These procedures provide you with the necessary steps to accomplish labs when using VHDL.*

Assumptions:

1. Students have a basic understanding of UNIX
2. Students know how to sign-into a UNIX environment from Windows NT

References: (a) "Force File and Force Commands", David Sendek, 9 July 2003
(b) ModelSim SE Tutorial Version 5.5e, 22 Aug 01, Mentor Graphics
(c) Lesson 2 – Basic VHDL Simulation, "Preparing the Simulation", Mentor Graphics, 22 Aug 01, pages T-18 to T-23

SETTING UNIX ENVIRONMENT (steps at the UNIX prompt)

1. (Suggestion) Create a directory ee451
2. (Suggestion) Create a sub-directory for each lab, ex: lab1 , lab2, …
3. **%setenv MGC_WD $HOME/*path***
   ex: %setenv MGC_WD $HOME/ee451/lab1
4. Change to your working lab sub-directory
5. **%source /mentor/csu_setup/ams_setup.csu**

Notes:

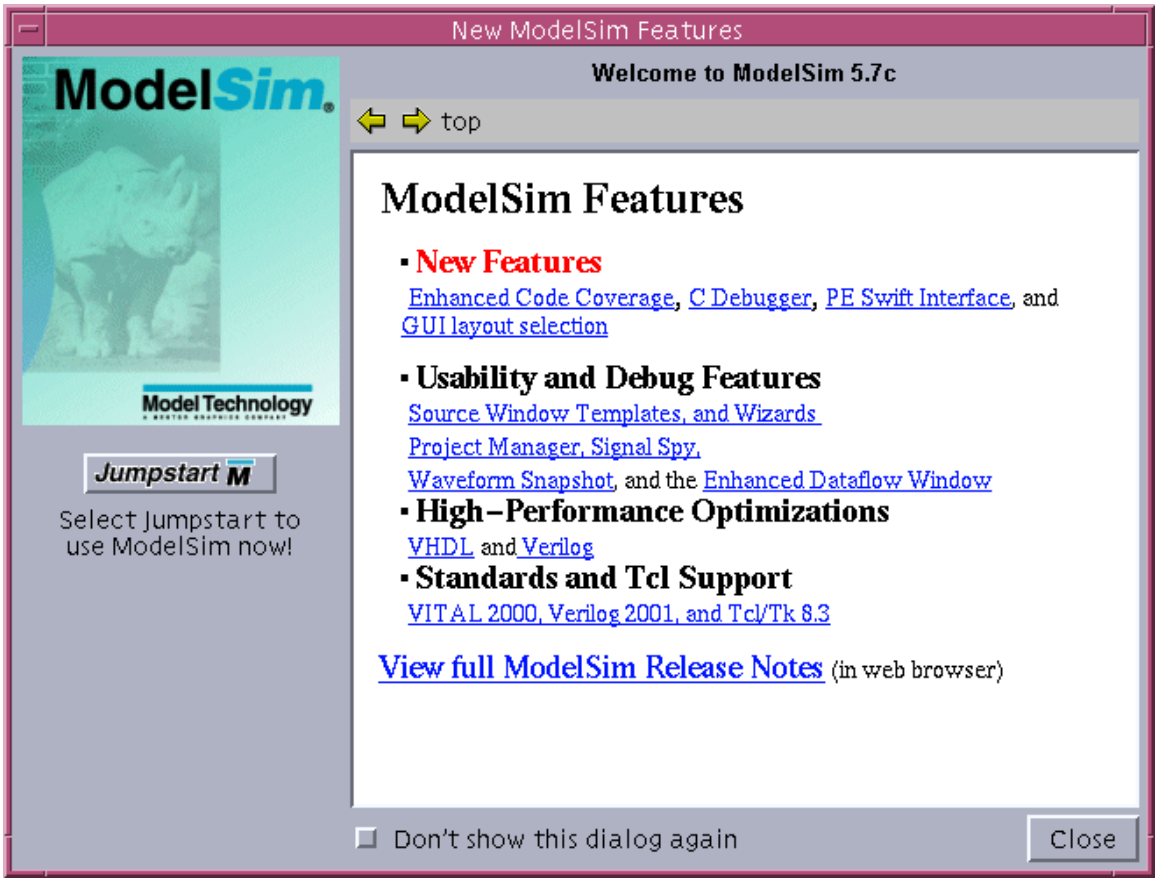
- This permits you to access ModelSim, used for compiling, linking and simulating VHDL source code.
- If you do not modify your .cshrc file, you must repeat steps 3 through 5 each time you re-open your UNIX window.
- There is a **space** between %source and /mentor….

Procedures:

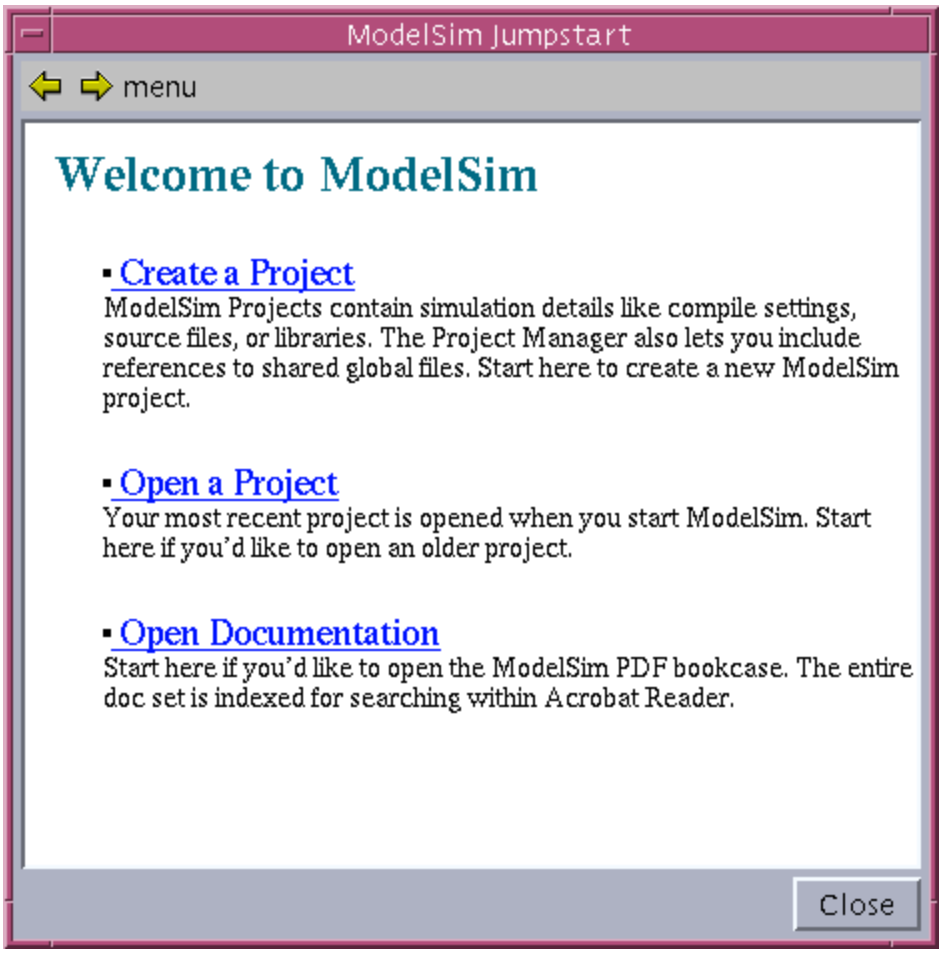
1. Using your favorite text editor, create the Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) source code for your design and a separate file with "force" commands to be used in simulating your design (if required). The force file is a set of test vectors to test your design. Reference (a) provides some force commands. Name the file such as "lab1.do"

2. From your /ee451/lab1 directory and at the Unix Prompt, start Mentor Graphics ModelSim by entering the following at the Unix prompt: qhsim

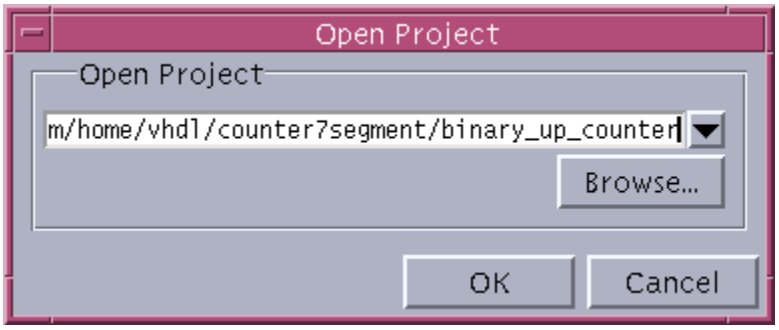
3. At the “Welcome to ModelSim 5.7” window, select “Jumpstart”.



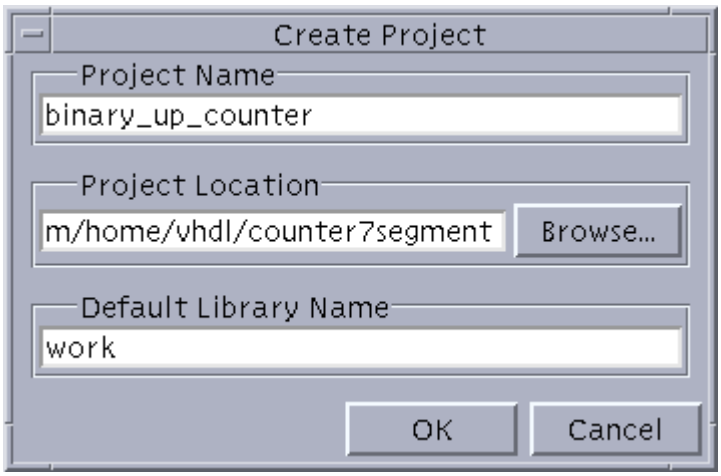
The following screen will be displayed. Select “Create a Project” or File > New > Project. Note: After you have initially created a project, future access to that project can be achieved by selecting “Open a Project”.



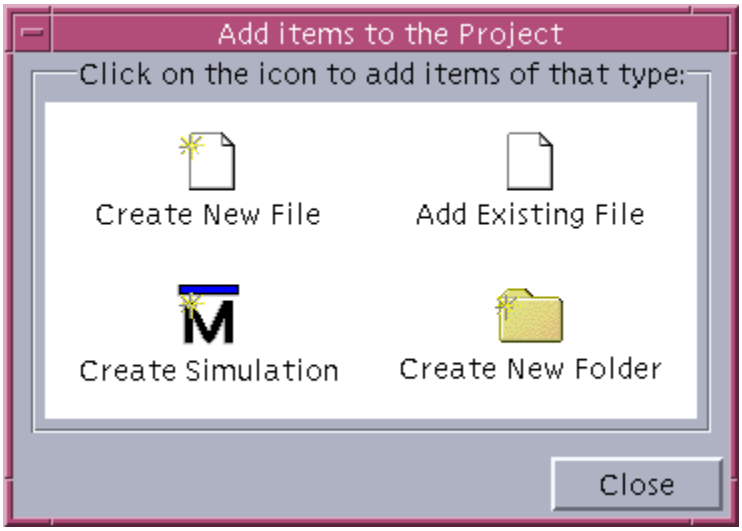
The following will be displayed if you have already created a project and want to open it at some later time. This will add the files that contain your design. You can then directly proceed to compiling your design.



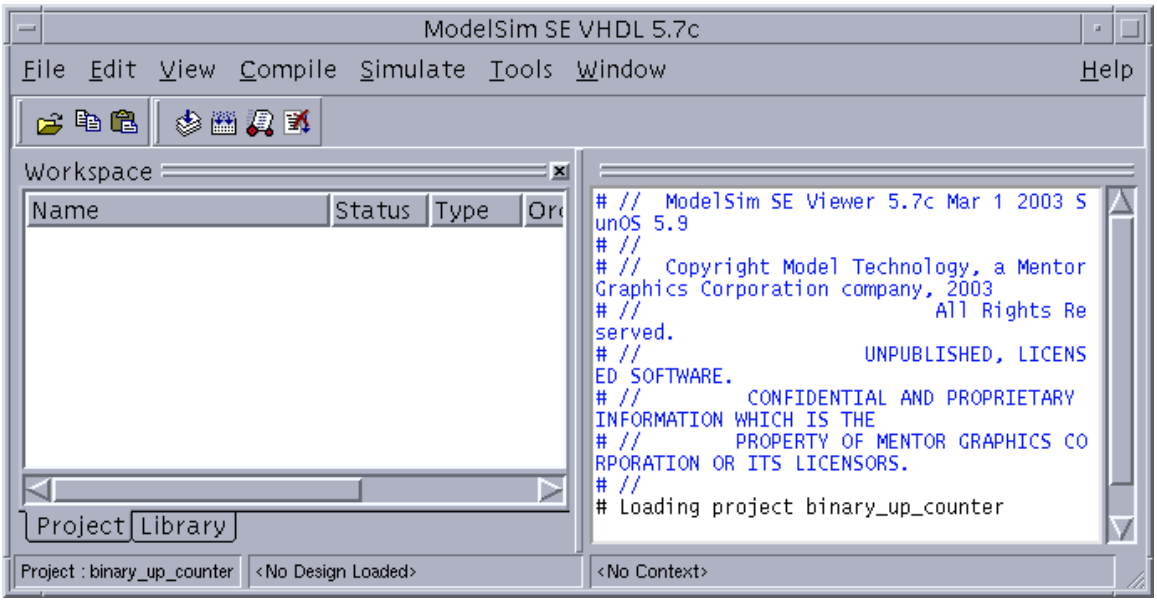
4. Before you compile any Hardware Design Language (HDL) (such as VHDL or Verilog), you'll need a design library to hold the compilation results. To create a new design library, type in the Project Name and select a directory where the project file will be stored. Leave the default library name set to "work". Finally, select OK.



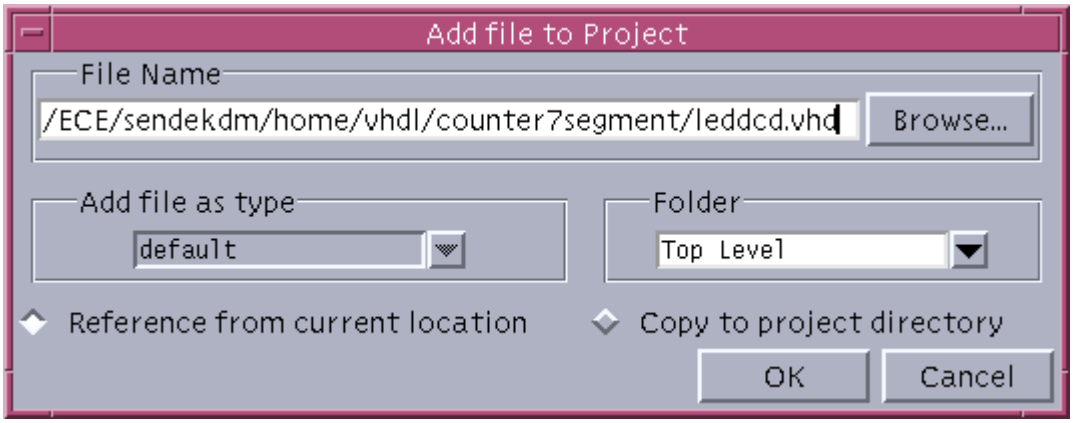
After pressing OK, the following will be displayed:



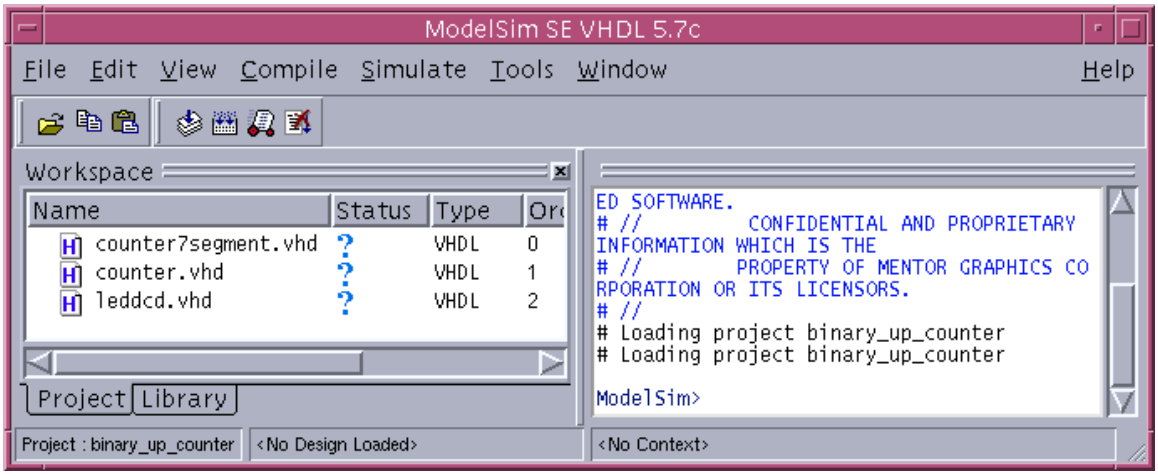
And your ModelSim main window will look like the following:



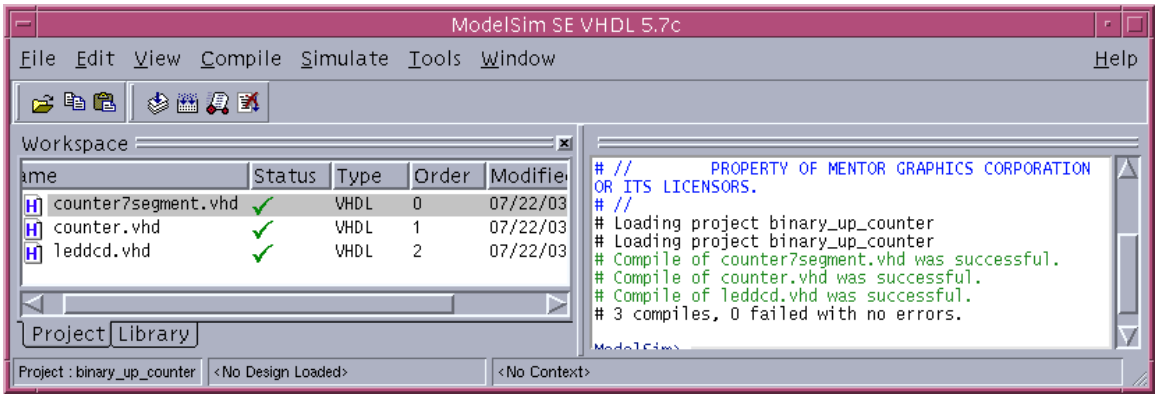
5. The next step is to add the files that contain your design. By now you would have written your VHDL source code file(s). Click "Add Existing File" in the "Add items to the Project" window. For this example, three VHDL files are added. Click the "Browse" button in the "Add file to Project". It should be noted that counter7segment.vhd, counter.vhd & leddcd.vhd are selected. Select "Reference from current location" and then click OK. Close the "Add items to the Project" dialog (This will close the "Add items to the Project" and "ModelSim Jumpstart" windows).

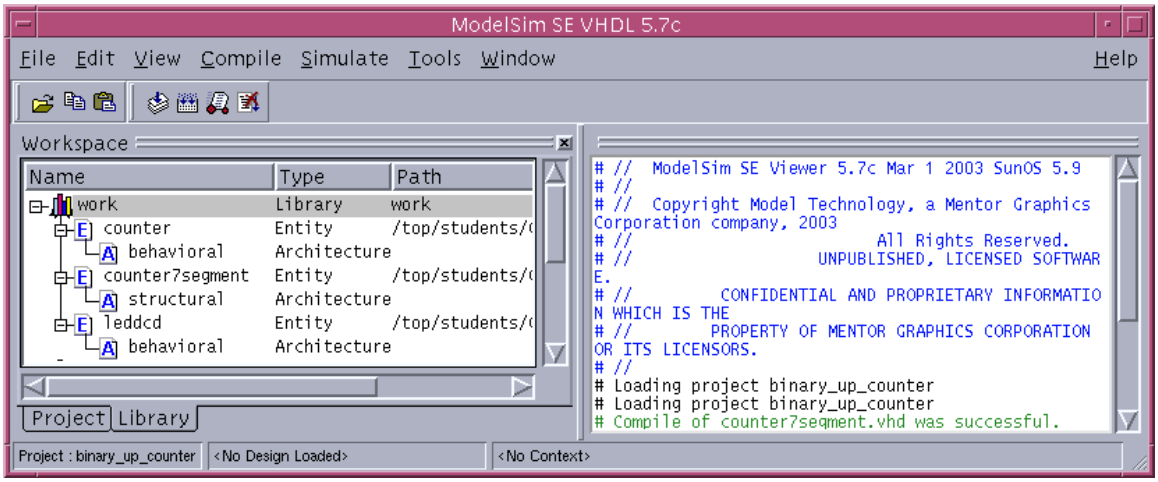


The main ModelSim window will show the following:



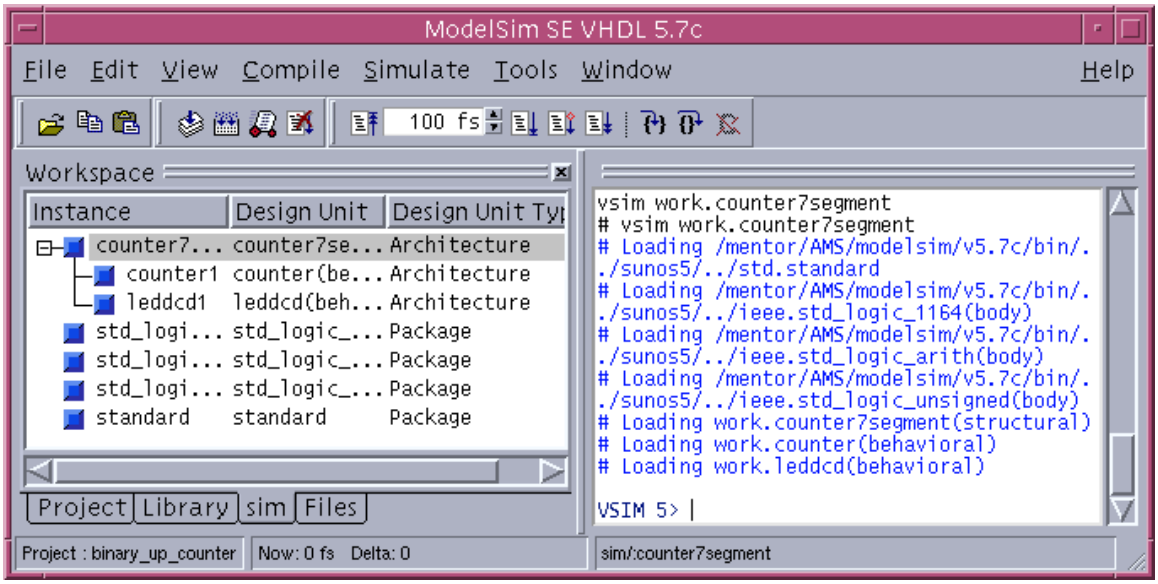
6. Now you are ready to compile the VHDL or Verilog file(s). To compile the file(s), select Compile > Compile All or highlight the "high-level" design (counter7segment.vhd in this example), right mouse click and select Compile > Compile All. By selecting the "Library" tab, you can observe the compiled design units (the Entity & Architecture blocks).



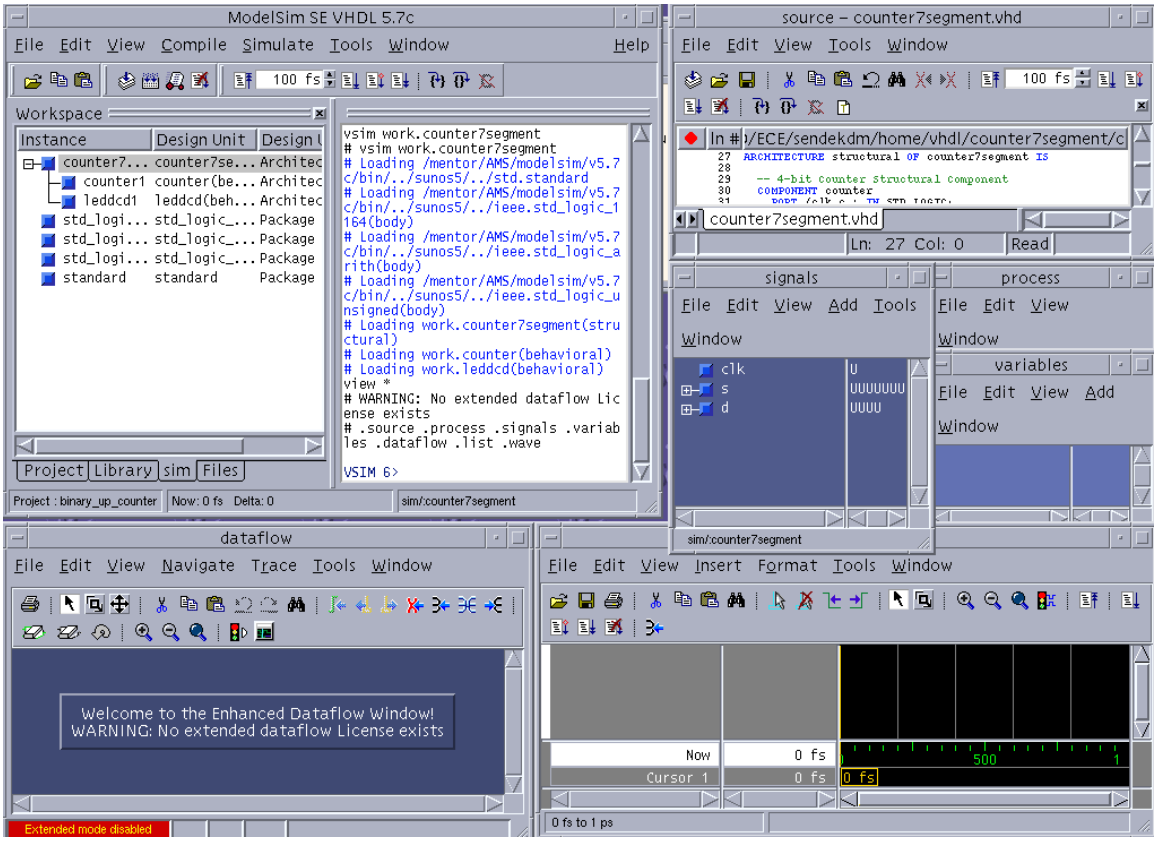


7. You may find compile errors in the previous step. These need to be corrected before proceding any further.

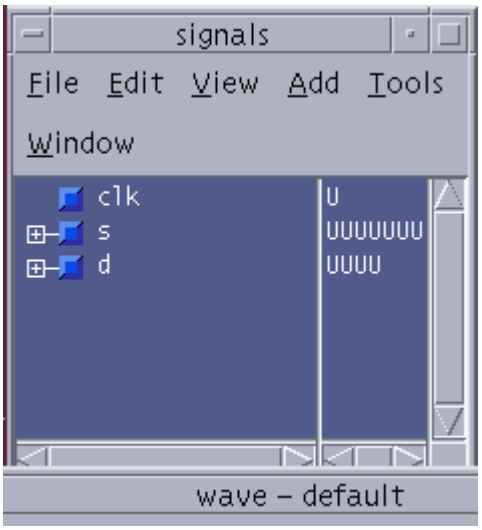
8. Now the design must be loaded, once compiled. Double-click the "high-level" design (counter7segment) on the Library page. You'll see a new page appear in the workspace that displays the structure of the counter7segment design unit.



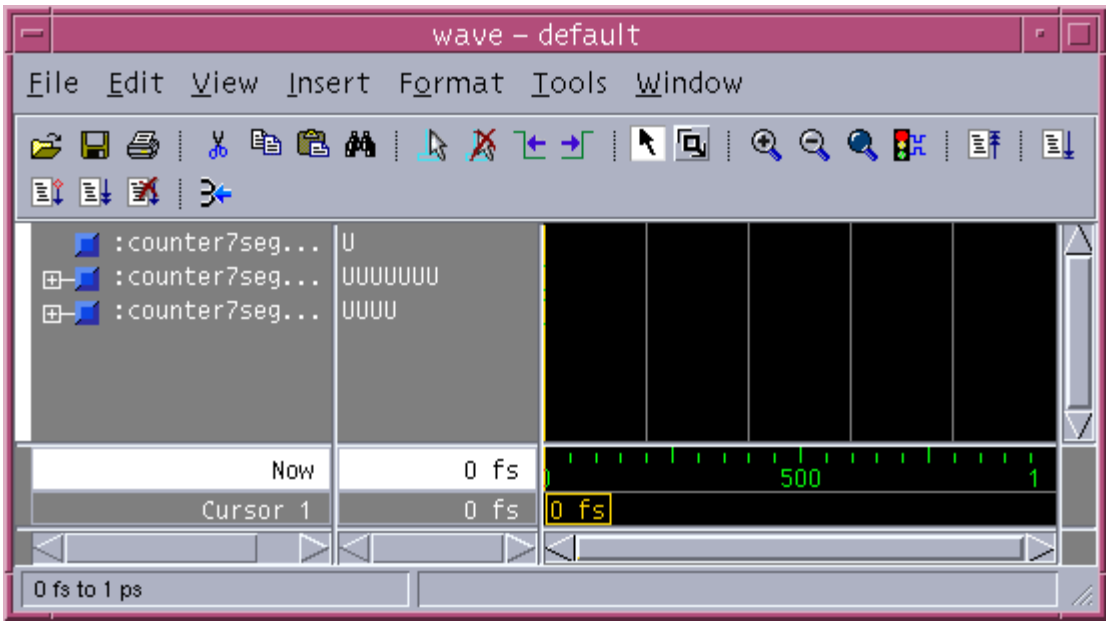
9. To simulate the design, select View > All Windows from the main ModelSim window. This will open all the ModelSim simulation windows, such as the wave window. This window will be what you will predominately use.



10. From the Signals window menu, select Add > Wave > Signals in Region. This command displays the top-level signals to the Wave window.

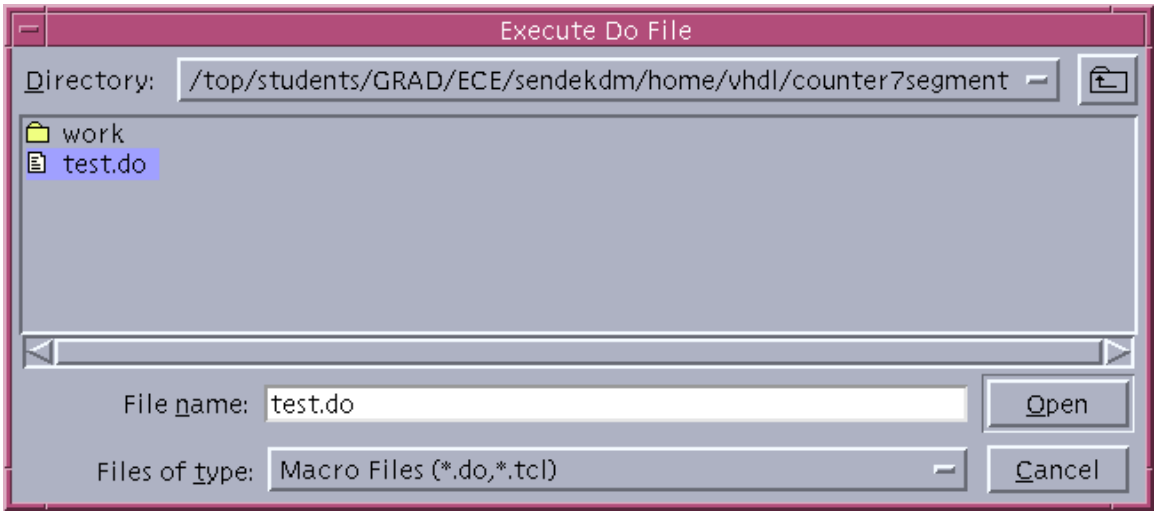


This will result in the following:

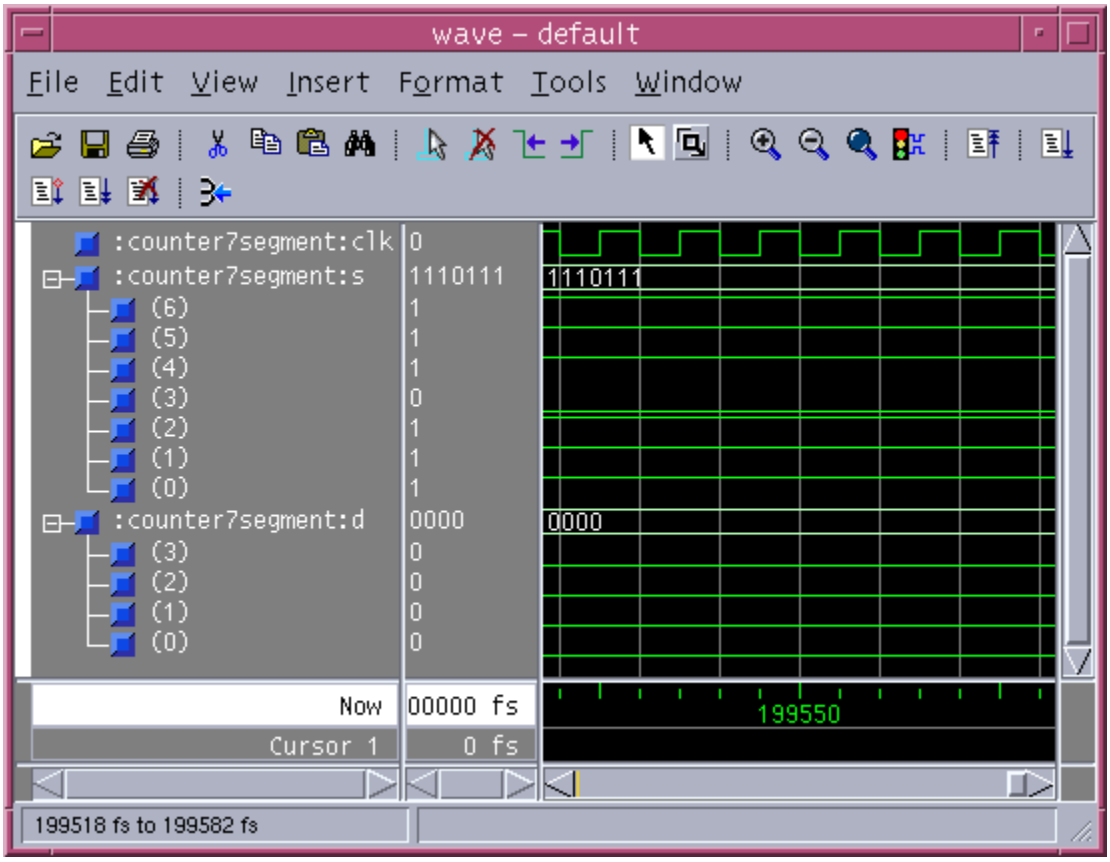


11. Of particular interest, if you are using a hierarchical design, the previous step only show the top-level signals. But if you require more detailed resolution, you can select from the signals window Add > Wave > Signals in Design.

12. Now you are ready to simulate your design. To simulate your design, you will use your test vectors that you placed in your force file. To execute your force file, to simulate your design, select Tools > Execute Macro from the main window menu. Finally, select the force file you created earlier. Note that a "force file" is also referred to as a "do" file.



A sample simulation may look like:



13. To exit ModelSim, select File > Quit in the main ModelSim window.

14. After simulation, you can use the XESS Field Programmable Gate Array (FPGA) protoboard to verify your design on physical hardware.

Useful Feature(s):

1. If you desire to clear your "wave" window during simulation, simply press the restart icon illustrated below.