

## ECE 332 Electronics Principles II

**Prerequisites:** ECE 331 with a grade of C or above.

**Course Credit:** 4 (Lecture and Lab)

**Instructor:** Tom Chen ([thomas.chen@colostate.edu](mailto:thomas.chen@colostate.edu))

**Lab TA:** Lang Yang ([yanqlang.shangze@gmail.com](mailto:yanqlang.shangze@gmail.com)) and  
Nick Grant ([nicholasgrant314@gmail.com](mailto:nicholasgrant314@gmail.com))

**HW Grader:** Devashish Vedre <[drv11291@gmail.com](mailto:drv11291@gmail.com)>

**Office:** Scott Building, Room 352

**Textbook:** Lecture notes (required) supplemented by “Fundamentals of Microelectronics” by Behzad Razavi (strongly recommended to own)

**Objectives:** This course is the continuation of Electronics I. It builds on the knowledge of device characteristics, models and operation in linear and non-linear circuits. This course will focus on basic analog circuits based on the MOS technology. BJT type circuits will not be covered in general. Progression of design concepts from simple, single stage linear circuits, to multi-stage linear circuits, to reference circuit, and output stages covers the basic set of design principles and guidelines. The learning will be further enforced by actual design projects students perform in the corresponding lab sessions and the knowledge integration modules. The design projects focus on design principles and verification of the designs with SPICE simulation results with the goal of understanding design tradeoffs.

**Assessments:** Two assessments (tests) are planned during the semester. Students can use any reference books, notes, and calculators to solve problems during the test period. Each assessment lasts a class period.

**Final Exam:** The final exam is open-book, open-notes. Use of calculators is allowed.

**Homework:** Homework assignments are posted online and they are due at 4pm on the day one week after the date of posting. A dropbox for all homework assignments is located inside the BC infill. Homework solutions will also be posted online.

**Laboratory:** 5-6 laboratory sessions are planned. All lab assignments are turned in to the TA. The lab report must follow the required format. Fail to do so will have a negative impact on your lab grade.

**Knowledge Integration:** There are three knowledge integration (KI) modules. Each KI module deals with a set of anchoring concepts taught in ECE312, ECE332, and ECE342 and shows how these concepts are integrated in a practical design. A set of questions related to the concepts used in each KI will be distributed before each KI module begins. Students are required to complete the pre-work in the form of a report by working through the questions and to understand how individual concepts are integrated in the practical design. Online presentations by each student to demonstrate his/her understanding of the materials in the first two KIs are required.

**Grading:**

- Laboratory 25%
- Homework 10%
- KI pre-work reports 5%
- KI presentations 5%
- Assessment I 15%
- Assessment II 15%
- Final exam 25%

**Note:**

No credit will be given to any lab work/report submitted after the solutions have been posted and discussed in the class. Thus, each student must complete all pre-laboratory assignments, attend lab sessions and submit a lab report. Lab reports must be done individually.

**Topics covered:**

1. Review of MOS transistor characteristics
2. CMOS silicon process overview
3. CMOS small signal model overview
4. CMOS current sources
5. CMOS common source circuit
6. CMOS common gate circuit
7. CMOS source follower (common drain circuit)
8. CMOS differential circuits
9. CMOS output stage design
10. CMOS OTA and Opamp
11. Frequency response of CMOS circuits
12. Principle of feedback structures
13. Stability analysis and compensation
14. Noise analysis

**Office Hours:**

Instructor office hours: MWF 11-noon or by appointment.

Instructor office telephone: 491 6574.

Instructor email address: [thomas.chen@colostate.edu](mailto:thomas.chen@colostate.edu)

Lab TAs are Lang Yang and Nick Grant. Any questions related to the labs should be directed to the lab TAs during any of the lab hours.

HW Grader is Devashish Vedre

The grader has office hours on Tuesdays and Fridays from 10:30-noon at the GA conference suite in Scott room 351. The best way to reach the grader is by email.