Lab 7

This is an individual design project. No grouping is allowed.

1. Use the multi-stage differential amplifier design obtained from your previous design project for this project. Add a resistive negative feedback to the circuit. You can use a variety of feedback topologies. When you add the feedback network, make sure that you don't drastically disturb the DC bias. Small changes may be necessary to the original circuit to maintain reasonable DC bias.
2. Simulate the circuit with the feedback and determine whether your circuit oscillates. Your circuit should not oscillate if you did Lab6 correctly.
3. Determine the closed loop gain in SPICE and compared it with the hand calculation result.

Design Project Report Requirement:

1. Discuss how you added the feedback network.
2. Provide the circuit schematic and the netlist with the feedback network.
3. Plot the frequency response of the close-loop gain. Mark the phase margin of the close-loop circuit.
4. Comments and conclusions.
5. Attach the SPICE netlist at the end of the report.

Circuit Submission Guideline:

Send an email to **your TA** with your name in the subject and your circuit in the body of the email. Make sure to send the email in plain text, not in html. The body of the email should be the same as the file used to run the test bench:

//Your name
//Your design area in "u" "p" "n", do not use E9 format, don't put the square meter in(6u)
//Your DC bias in the unit of mV (i.e. 700m)

subckt AMP vdd vss inp inn out

Your circuit with just fets cap and resistors, and the ports name should exactly be the same as previous line (vdd vss inp out, all in small characters)