Lab 6

This is an individual design project. No grouping is allowed.

1. Use the multi-stage differential amplifier design obtained from your previous design project for this project. Add a compensation capacitor to the circuit to obtain the phase margin of 60 degrees.

Design Project Report Requirement:

1. Discuss where you choose to add the compensation capacitor by providing the phase margin before and after you added the compensation capacitor.
2. Provide the circuit schematic and the netlist with the miller compensation capacitance.
3. Plot the frequency response of the circuit with and without the compensation capacitor. Mark the phase margin of the circuit.
4. Comments and conclusions.
5. Attach the SPICE netlist at the end of the report.

Circuit Submission Guideline:

Send an email to **Your TA** with your name in the subject and your circuit in the body of the email. Make sure to send the email in plain text, not in html. The body of the email should be the same as the file used to run the test bench:

//Your name
//Your design area in "u" "p" "n", do not use E9 format, don't put the square meter in(6u)
//Your DC bias in the unit of mV (i.e. 700m)

subckt AMP vdd vss inp inn out

Your circuit with just fets cap and resistors, and the ports name should exactly be the same as previous line (vdd vss inp out, all in small characters)