

Lab 5

This is an individual design project. No grouping is allowed.

1. Convert your differential amplifiers in your previous design project to folded differential amplifiers and add common mode feedback circuit to all differential amplifiers in your design. You can use an ideal voltage source for Vref input for the desired common mode feedback. Design the circuit to keep the original specs from the last design project.
2. Perform frequency response (both amplitude and phase) for the new circuit with folded diff stages and common mode feedback. Plot the frequency response curves.
3. **This is optional!** You can earn up to 20% bonus points if you can show that you have changed your design (either size or topology, or both) in such a way to increase bandwidth of the circuit. The amount of bonus points given depend on the amount of bandwidth you have improved.

Design Project Report Requirement:

1. Provide circuit schematic for your design.
2. Discuss your design of folded differential amplifiers with common mode feedback. Going through your design process to list the pros and cons of the design choices you made in this design.
3. Discuss your choice of the desired common mode output voltage used in the common mode feedback circuit and why.
4. Provide the circuit schematic and the frequency response plots.
5. Discuss the results of the frequency response from SPICE simulations. List the number of poles and zeros reported by SPICE and identify them on the frequency response plots in your report.
6. Comments and conclusions.
7. Attach the SPICE netlist at the end of the report.

Circuit Submission Guideline:

Send an email to your lab TA with your name in the subject and your circuit in the attachment of the email. Make sure to send the email in plain text. The body of the email should be the same as the file used to run the test bench:

//Your name

//Your design area in “u” “p” “n”, do not use E9 format, don't put the square meter in(6u)

//Your DC bias in the unit of mV (i.e. 700m)

subckt AMP vdd vss inp inn out

Your circuit with just fets cap and resistors, and the ports name should exactly be the same as previous line (vdd vss inp out, all in small characters)

ends AMP

I8 (vdd! 0 net5 net09 net1) AMP

V0 (vdd! 0) vsource dc=1.8 type=dc

V2 (0 net09) vsource dc=-y mag=s ampl=s type=sine freq=1M

V1 (net5 0) vsource dc=y mag=s ampl=s type=sine freq=1M

R0 (net1 0) resistor r=1K