

Lab 4

This is an individual design project. No grouping is allowed.

Design an operational amplifier with a differential input and a single-ended output. It must meet the following specifications:

Lmin	0.18um
Wmin,nmos	0.22um
Wmin,pmos	0.22um
Vdd	1.8V
Vss	0V
R load	1 Kohms
Adm (Vout/Vid)	>1000
Acm (Vout/Vic)	<1
Vicm,max-Vicm,min	>300mV
Vout,p-p	>600mV

The design goal is to meet all the design specs. The available circuit components are NMOS transistors, PMOS transistors, and resistors. (Ideal internal sources cannot be used to generate bias currents or voltages.)

For hand calculation, use the following parameters:

$$K'_{nmos} = 140 \mu A / V^2$$

$$K'_{pmos} = 52 \mu A / V^2$$

$$V_{t,nmos} = 550 mV$$

$$V_{t,pmos} = -550 mV$$

$$\lambda_{nmos} = 0.18$$

$$\lambda_{pmos} = 0.16$$

$$\alpha_{nmos} = 1.15$$

$$\alpha_{pmos} = 1.37$$

The total area of the design will be approximated by adding up the gate area (W*L) for all the transistors in the circuit. The figure of merit for the design will be power*gate_area. For the resistors, the material's sheet resistance is 250Ohm/square with the minimum width of 0.5um. In the FOM calculation, you need to include the area for resistors.

Design Project Report Requirement:

1. Discussion of your topology choice: explain why you chose a certain topology and compare your topology with possible alternatives.
2. Discussion of your sizing and area minimization strategy: explain how you chose all the W's, L's, V_{dsat} 's and currents; show your hand calculations.
3. A schematic (drawn by hand) of your circuit, annotated with all the node voltages.
4. Provide a table with W, L, V_{dsat} and I_{ds} for every transistor. For V_{dsat} and I_{DS} , include both the calculated and the simulated values. You only need to add one entry for every pair of symmetric transistors, such as the transistors in a differential pair.
5. Provide simulation results and waveforms showing the results.
6. Comments and conclusions.
7. Attach the SPICE netlist at the end of the report.

Circuit Submission Guideline:

Send an email to your TA with your name in the subject and your circuit in the body of the email. Make sure to send the email in plain text, not in html. The body of the email should be the same as the file used to run the test bench:

```
.param VIC = < your midpoint of the common mode input range >  
.subckt amplifier inp inn out vdd vss  
< your circuit >  
.ends
```

The subcircuit should be named 'designproject1' and the order of the input nodes should be: input node, output node, Vdd supply, Vss supply. You can change the names of the nodes.