Lab #3

This is an individual design project. No grouping is allowed.

Design a single-transistor common source/common drain CMOS amplifiers using TSMC's 0.18um CMOS process to maximize voltage gain. The load for the amplifier is a 1MOhms resistor. You can only use NMOS, PMOS, and resistors in your circuit. Ideal voltage sources can only be used for the supply voltage. No ideal sources are allowed for bias. Once the design for the 1MOhms is completed, now switch the load to 500 Ohms and check the overall design. Adjust the design in this case to better meet the design goal.

For hand calculation, use the following parameters:

$K'_{nmos} = 167\ uA/V^2$

$K'_{pmos} = 50uA/V^2$

$V_{t,nmos} = 563mV$

$V_{t,pmos} = -630mV$

$\lambda_{nmos} = 0.1$

$\lambda_{pmos} = 0.043$

The total area of the design will be approximated by adding up the gate area (W*L) for all the transistors in the circuit. The figure of merit for the design will be (voltage gain)/(power*gate_area). For the resistors, the material's sheet resistance is 250Ohm/square with the minimum width and length of 0.5um. The design specifications are listed in the following table:

Lmin	0.18um
Wmin,nmos	0.22um
Wmin,pmos	0.22um
Vdd	1.8V
Vss	0V
R load	1MOhms, & 500 Ohms
Vin, DC	0.7-1.0V
Vout,DC	0.7-1.0V
Av	As high as you can make it to be!
Power consumption	As low as possible
Total gate area	As small as possible

Design Project Report Requirement:

1. Discussion of your sizing and area minimization strategy for both designs: explain how you chose all the W's, L's, V_{Dsat}'s and currents; show your hand calculations.
2. A schematic (drawn by hand) of your circuit, annotated with all the node voltages.
3. Provide a table with W, L, VDsat and IDS for every transistor for both designs. For V_{Dsat} and I_{DS}, include both the calculated and the simulated values. You only need to add one entry for every pair of symmetric transistors, such as the transistors in a differential pair.
4. Provide simulation results and waveforms showing the results.
5. Comments and conclusions for both designs.
6. Attach the SPICE netlist at the end of the report.

Circuit Submission Guideline:

Send an email to **your lab TA with** your name in the subject and your circuit in the body of the email. Make sure to send the email in plain text, not in html. The body of the email should be the same as the file used to run the test bench:

.subckt amplifier inp outp vdd
vss < your circuit >
.ends

The subcircuit should be named 'designproject1_1mhoms' and 'designproject1_500ohms', and the order of the input nodes should be:
input pin, output pin, Vdd supply, Vss supply. You can change the names of the nodes.