Lab #2

Design a simple current source. The output of the current source is connected to a voltage source whose voltage can be swept during simulation. The circuit is designed in TSMC 0.18um CMOS process. The nominal output current for the current source should be 50uA. The rest of the specs are:

1. The output impedance should be above 100KOhm
2. All bias circuits for the current source should be included as shown in the diagram below.
3. The current mismatch of the current source should be below 15%.
4. The output compliance voltage, defined as the minimum output voltage to keep the output impedance above 100KOhm, should be at least 400mV.
5. Use simulations to show the output impedance of the current source
6. Use Monte Carlo simulations to show the current source output mismatch is within 15% of its nominal output
7. Use K'_nmos=330uA/V^2 and K'_pmos=61uA/V^2 for hand calculation
8. Use Vt_nmos=480mV and Vt_pmos=460mV for hand calculation

When the HW is due, you need to submit the following:

1. Show all 1st order hand calculations for determining transistor sizes, output impedance, and output compliance requirement.
2. Schematics with transistor W and L values clearly marked
3. Simulation results to show
    a. Output impedance,
    b. Output compliance,
    c. Output mismatch
4. Discussions about the design choices and reasons for choosing the transistor sizes in the design