MC74HC173

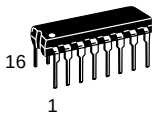
Quad 3-State D Flip-Flop with Common Clock and Reset

High–Performance Silicon–Gate CMOS

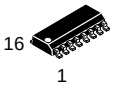
The MC74HC173 is identical in pinout to the LS173. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data, when enabled, are clocked into the four D flip–flops with the rising edge of the common Clock. When either or both of the Output Enable Controls is high, the outputs are in a high–impedance state. This feature allows the HC173 to be used in bus–oriented systems. The Reset feature is asynchronous and active high.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity 208 FETs or 52 Equivalent Gates



N SUFFIX
PLASTIC PACKAGE
CASE 648–08

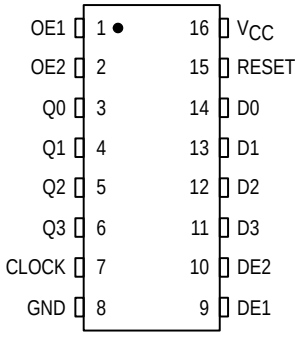


D SUFFIX
SOIC PACKAGE
CASE 751B–05

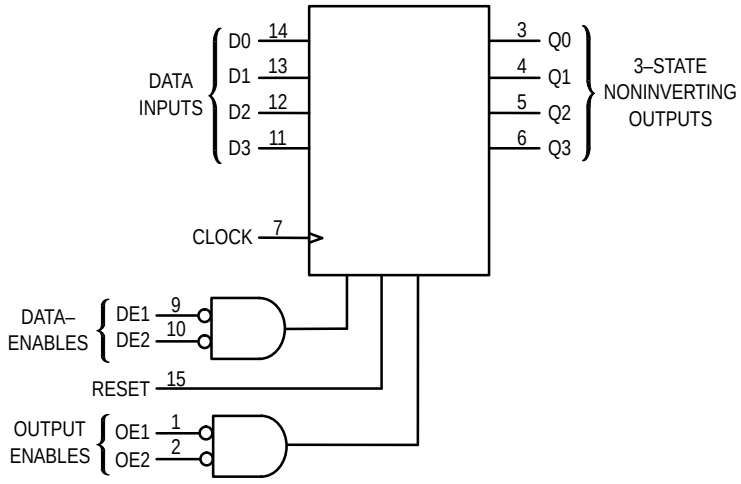
ORDERING INFORMATION

MC74HCXXXN	Plastic
MC74HCXXXD	SOIC

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

Inputs							Output
Output Enables				Data Enables		Data	
OE1	OE2	Reset	Clock	DE1	DE2	D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	No Change
L	L	L	H	X	X	X	No Change
L	L	L	↑	H	X	X	No Change
L	L	L	↑	X	H	X	No Change
L	L	L	↑	L	L	L	L
L	L	L	↑	L	L	H	H
L	L	L	↓	X	X	X	No Change
L	H	X	X	X	X	X	High Impedance
H	L	X	X	X	X	X	High Impedance
H	H	X	X	X	X	X	High Impedance